Reversible MOS chips

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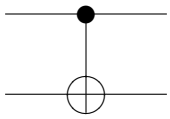
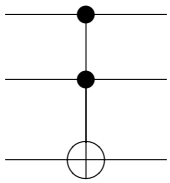
Workshop topics addressed :

6. Design priciples in MOS circuits

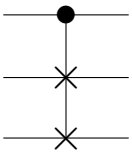
8. Classical mode (i.e. not quantum mode)
. of MOS reversible computing



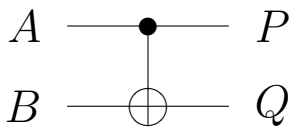
FEYNMAN **gate**



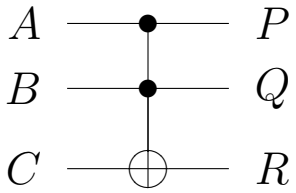
TOFFOLI **gate**



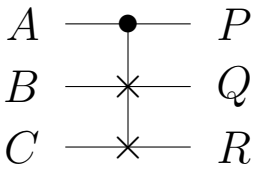
FREDKIN **gate**



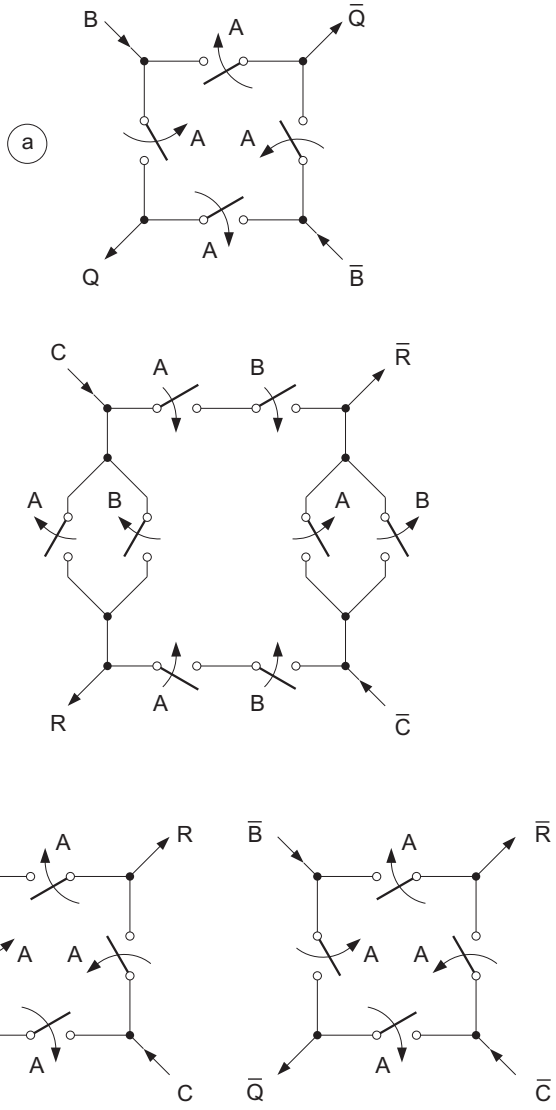
FEYNMAN gate



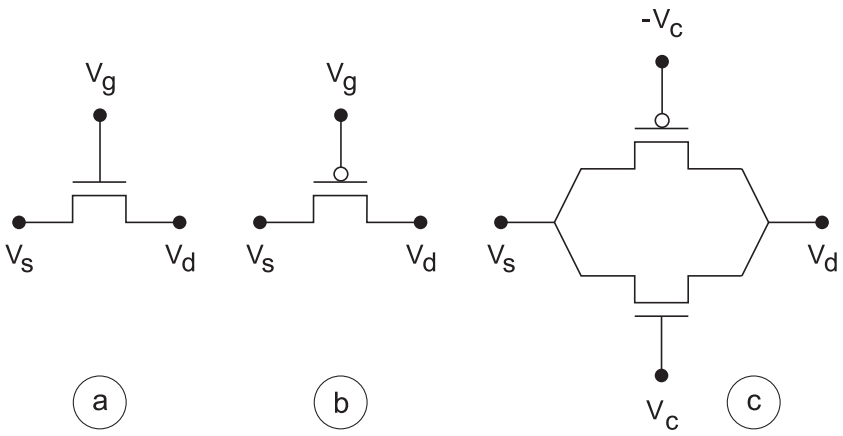
TOFFOLI gate



FREDKIN gate



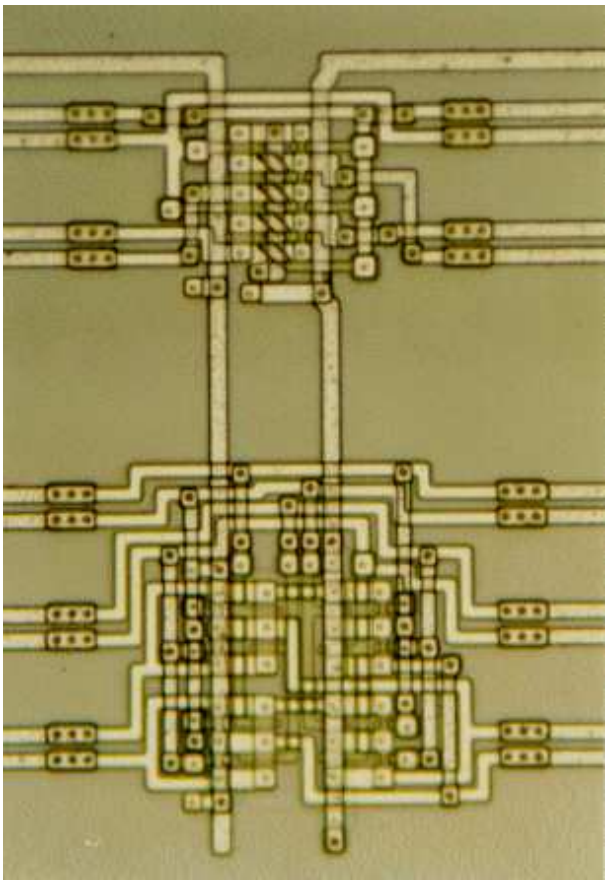
Implementation of
(a) `FEYNMAN` gate
(b) `TOFFOLI` gate
(c) `FREDKIN` gate.



A witch in MOS consists of

(a) an n-type MOS transistor and
(b) a p-type MOS transistor,

(c) together a ‘transmission gate’.



Microscope photograph (24 μm $\times$ 36 μm) of `FEYNMAN` gate and `TOFFOLI` gate (8 and 16 transistors, respectively).

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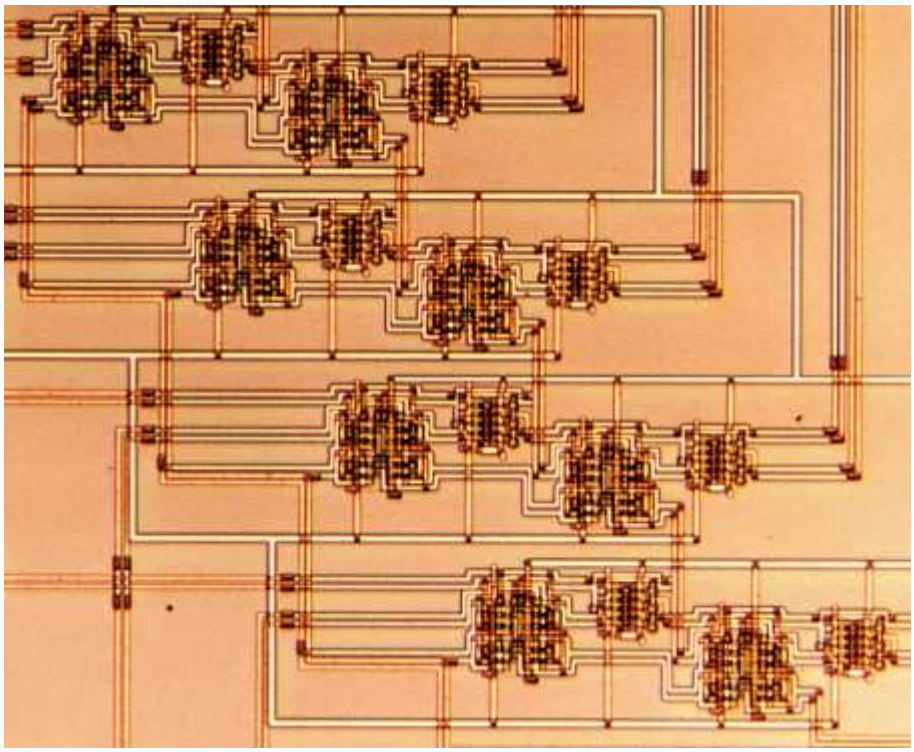

Microscope photograph (140 μm $\times$ 120 μm) of 2.4-μm 4-bit reversible ripple adder (192 transistors).

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Microscope photograph (140 μm $\times$ 230 μm) of 0.35-μm 8-bit Cuccaro adder (392 transistors).

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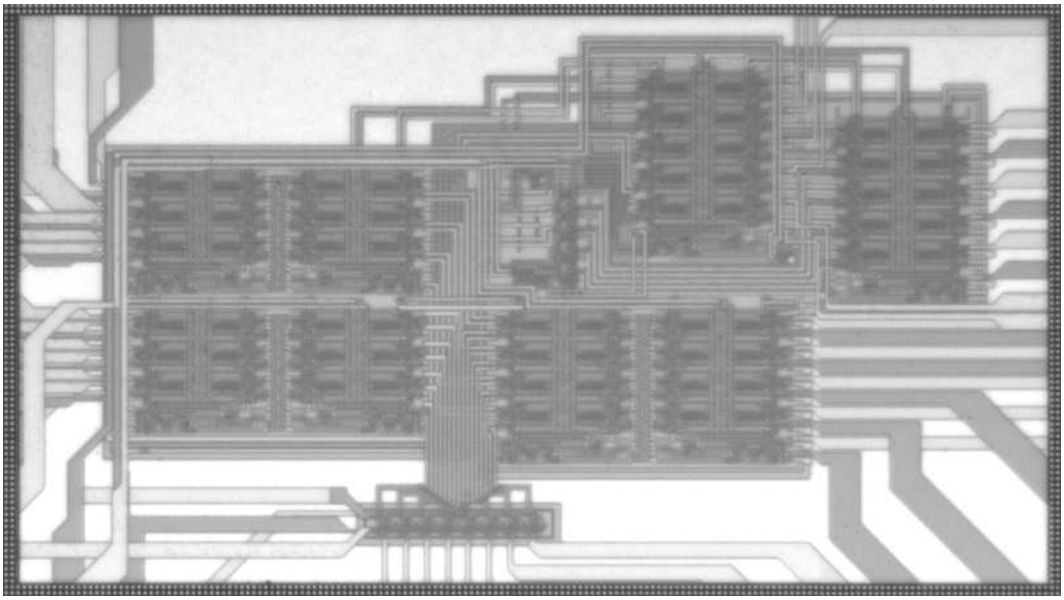

Microscope photograph (680 μm $\times$ 380 μm) of 0.35-μm 4-data H.264 transform (1,648 transistors).

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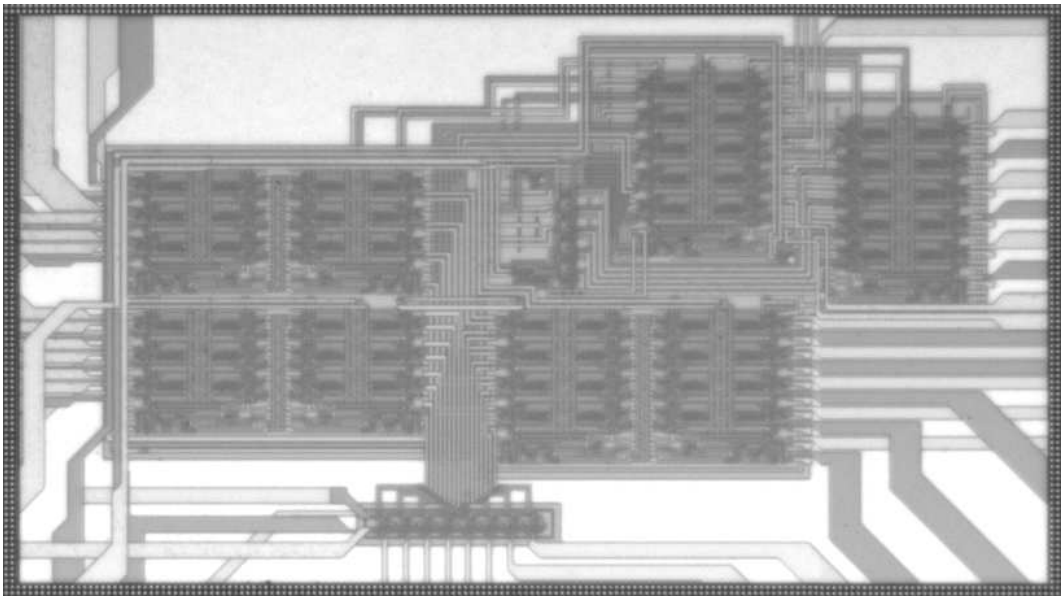

Microscope photograph (680 μm $\times$ 380 μm) of 0.35-μm 4-data H.264 transform (1,648 transistors).

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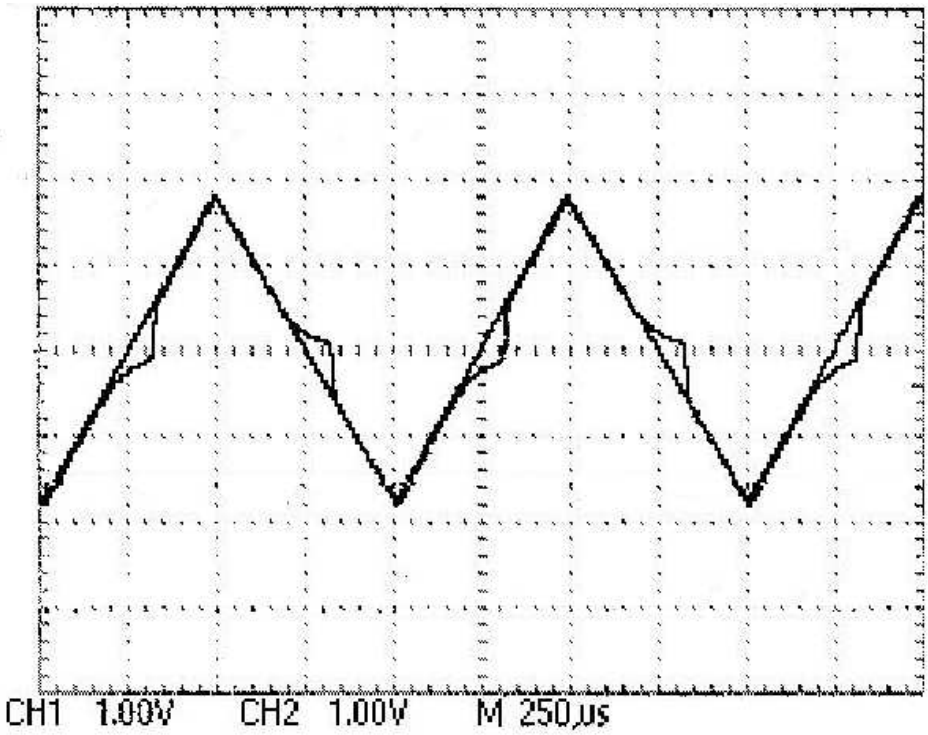
$$\begin{pmatrix} \mathbf{P} \\ \mathbf{Q} \\ \mathbf{R} \\ \mathbf{S} \end{pmatrix} = \begin{pmatrix} \mathbf{1} & \mathbf{1} & \mathbf{1} & \mathbf{1} \\ \mathbf{2} & \mathbf{1} & \mathbf{-1} & \mathbf{-2} \\ \mathbf{1} & \mathbf{-1} & \mathbf{-1} & \mathbf{1} \\ \mathbf{1} & \mathbf{-2} & \mathbf{2} & \mathbf{-1} \end{pmatrix} \begin{pmatrix} \mathbf{A} \\ \mathbf{B} \\ \mathbf{C} \\ \mathbf{D} \end{pmatrix}$$



Oscilloscope view of 0.35 μm full adder.

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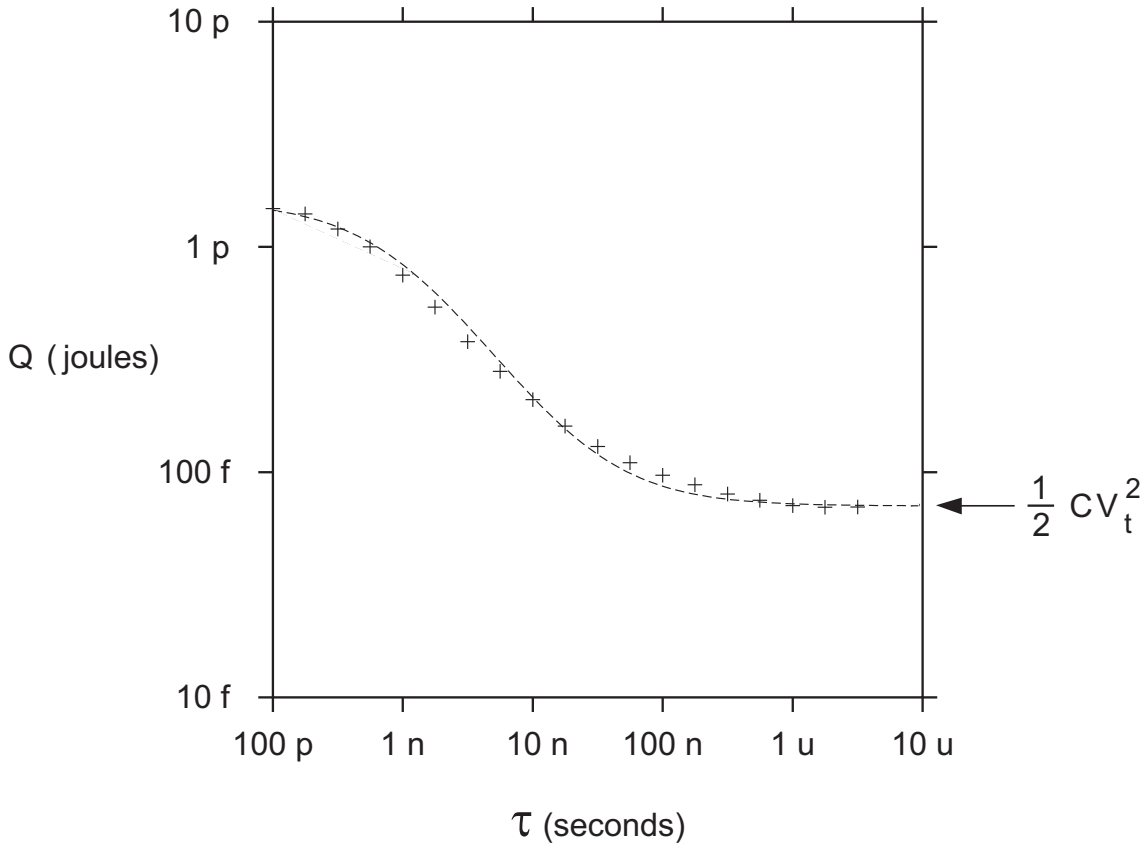
$$Q \approx CV^2$$

$$Q \approx \frac{RC}{\tau} CV^2$$



Moore's law for
dimensions L, W, and t
threshold voltage V_t
heat dissipation Q

technology (μm)	L (μm)	W (μm)	t (nm)	V_t (V)	Q (f J)
2.4	2.4	2.4	42.5	0.9	38
0.8	0.8	2.0	15.5	0.75	2.0
0.35	0.35	0.5	7.4	0.6	0.30
0.13	0.12	0.16	3	0.35	0.03

Energy dissipation per computational step:

$$Q \approx \frac{1}{2}\, C V_t^2 \ ,$$

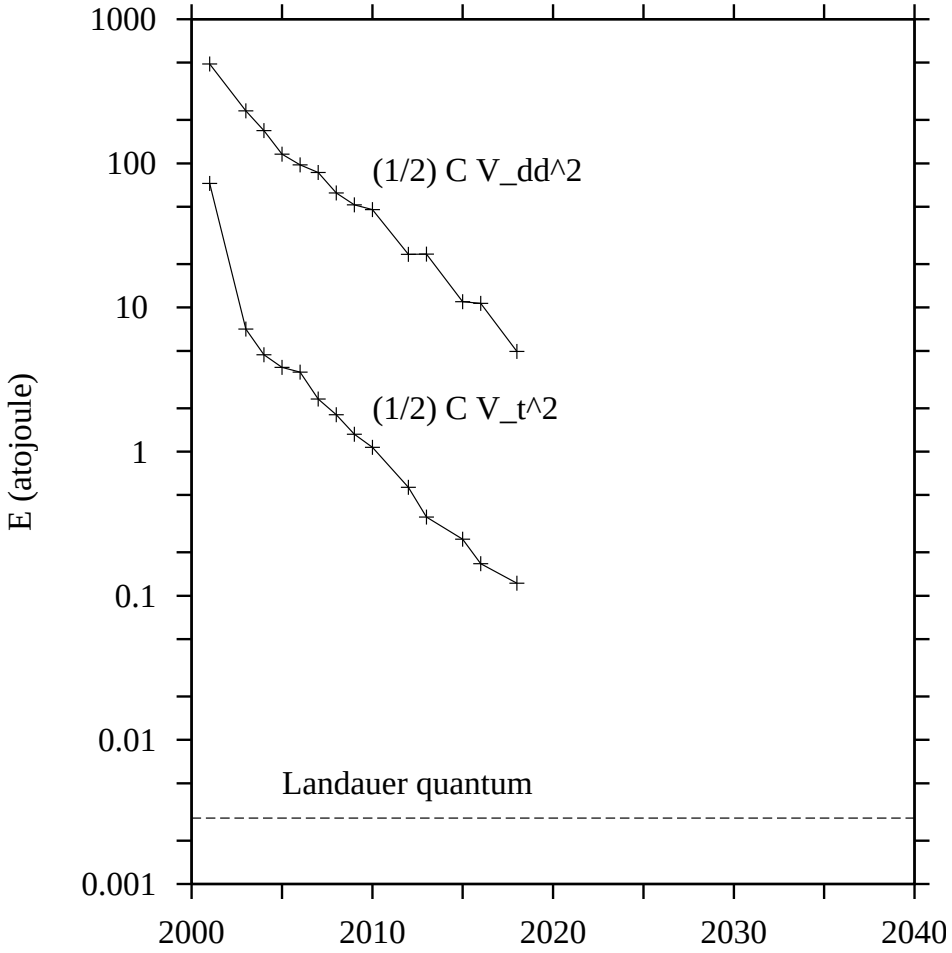
where

$$C \approx \epsilon_0\, \epsilon\, \frac{W L}{t}$$

We compare with the Landauer quantum

$$kT \log(2) \approx 3 \ \mathbf{z\,J} = \mathbf{0.000\ 003\ f\,J} \ .$$

C = **transistor capacitance**
V_{dd} = **power-supply voltage**
V_t = **transistor threshold voltage**



A perspective from the 2003 ITRS
= International Technology Roadmap of Semiconductors.

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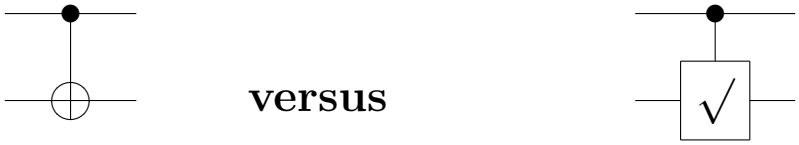
From classical reversible to quantum ?

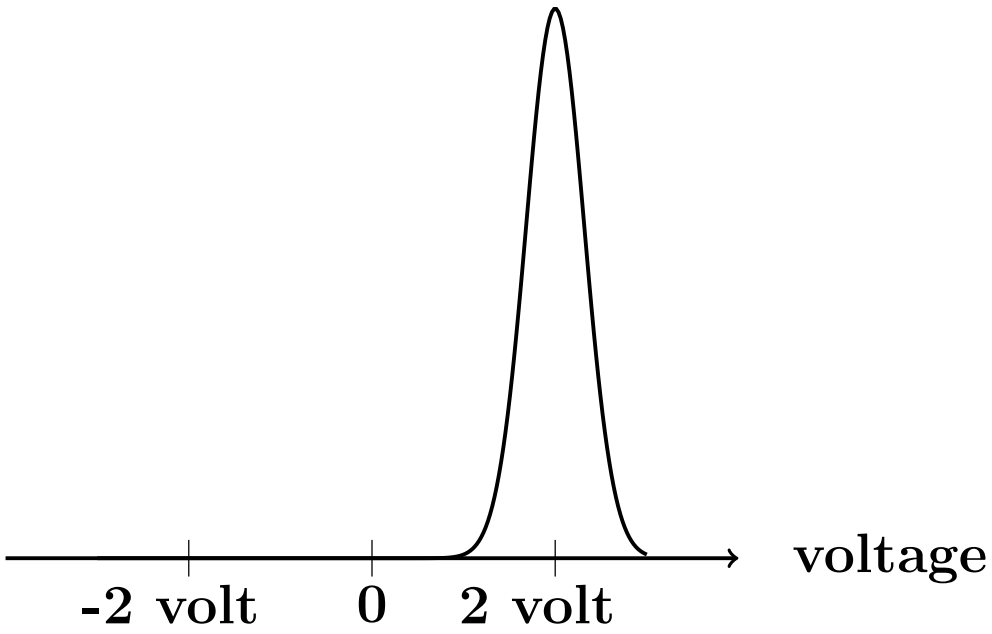
From classical reversible to quantum ?

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \quad \text{versus} \quad \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1/2+\mathrm{i}/2 & 1/2-\mathrm{i}/2 \\ 0 & 0 & 1/2-\mathrm{i}/2 & 1/2+\mathrm{i}/2 \end{pmatrix}$$

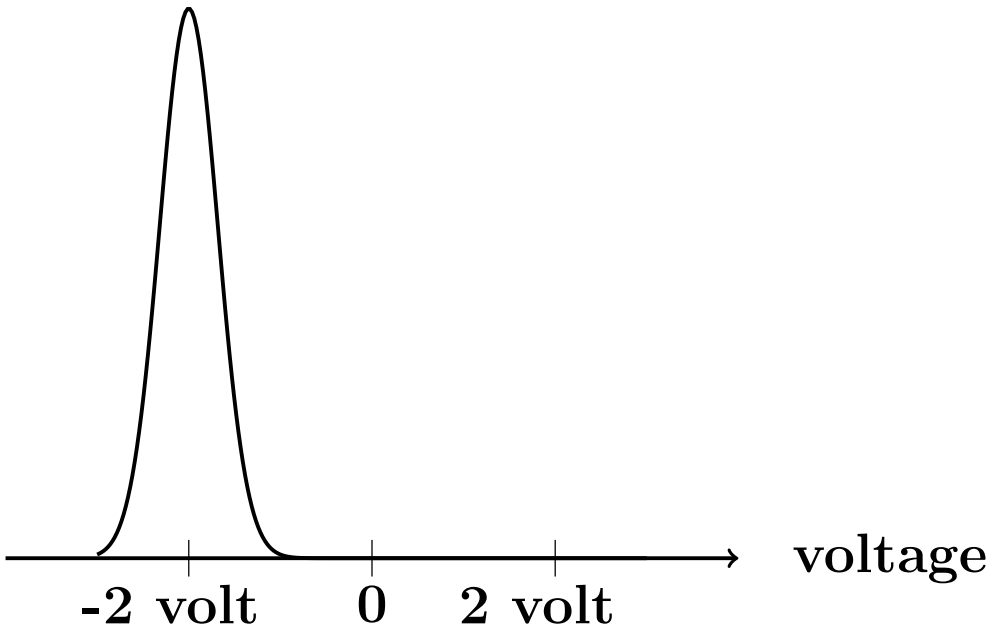
with respective symbols

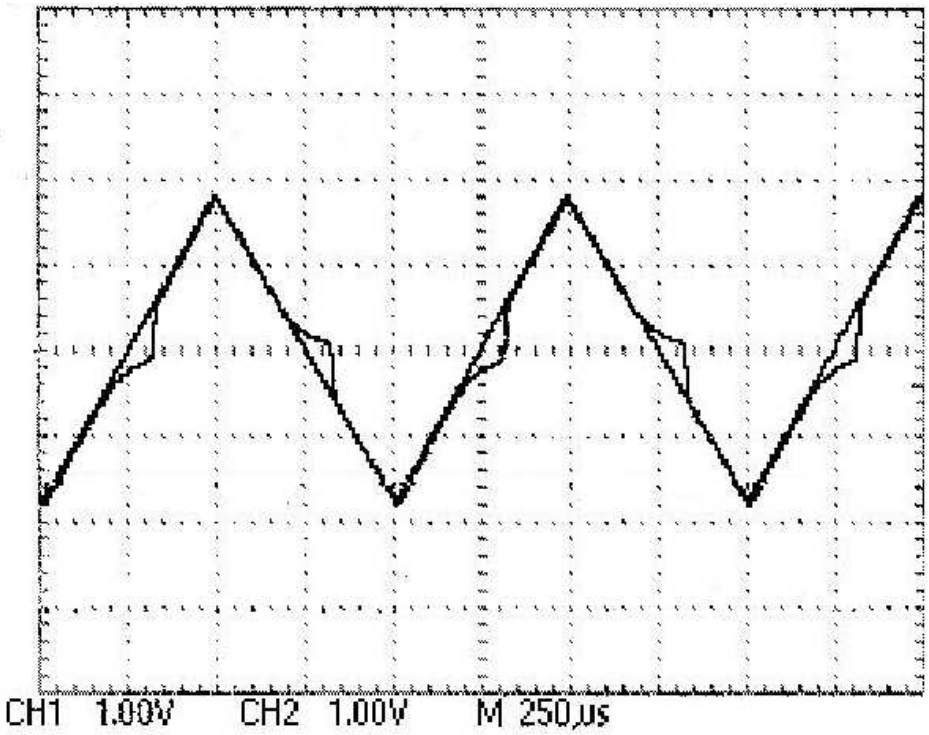


Probability distribution for logic 1



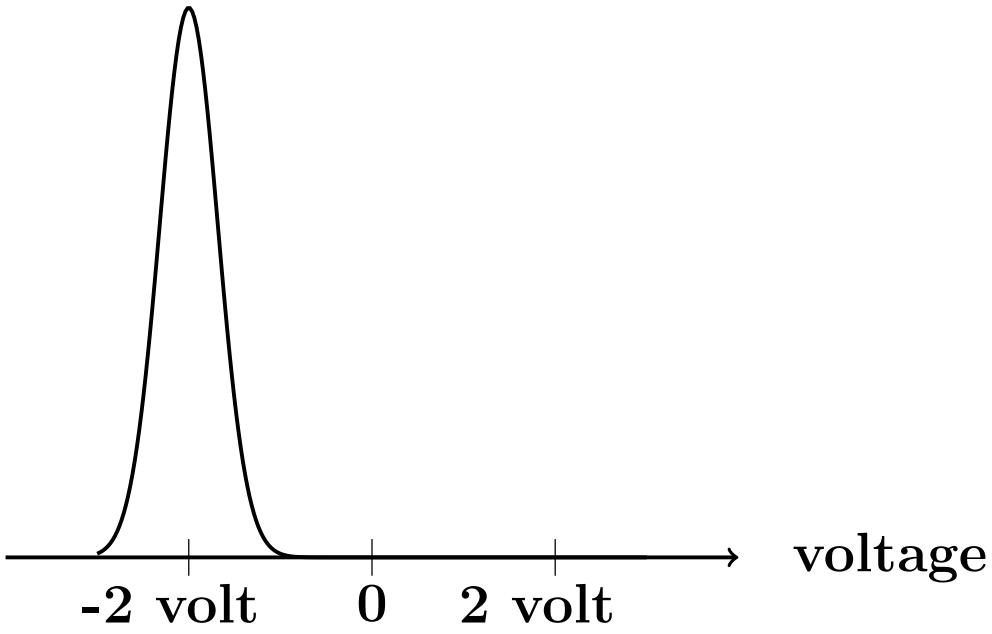
Probability distribution for logic 0




CH1 1.00V
CH2 1.00V
M 250µs

.

Probability distribution during classical transition from logic 0 to logic 1



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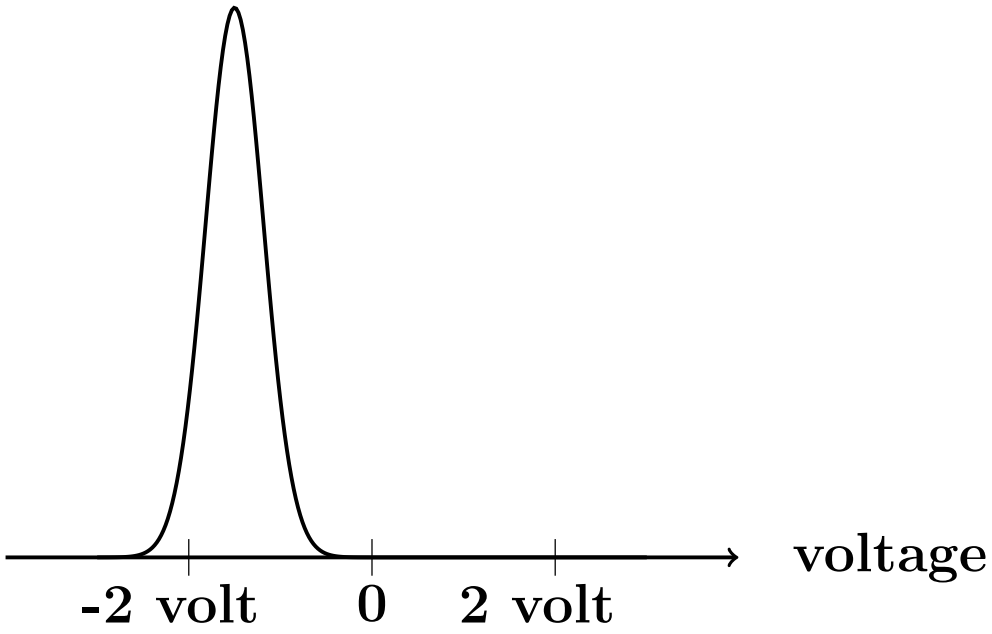

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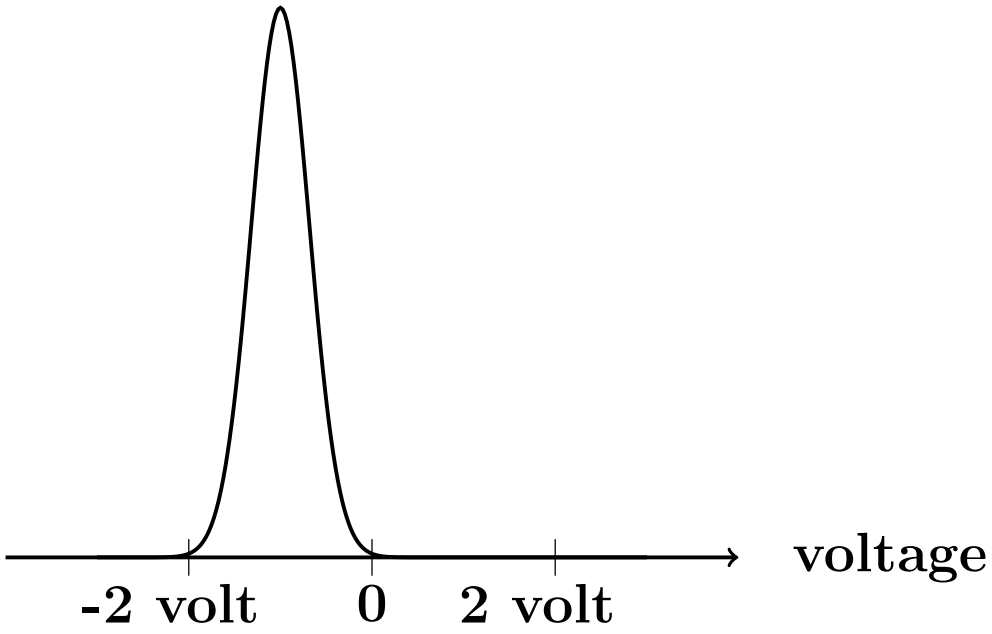

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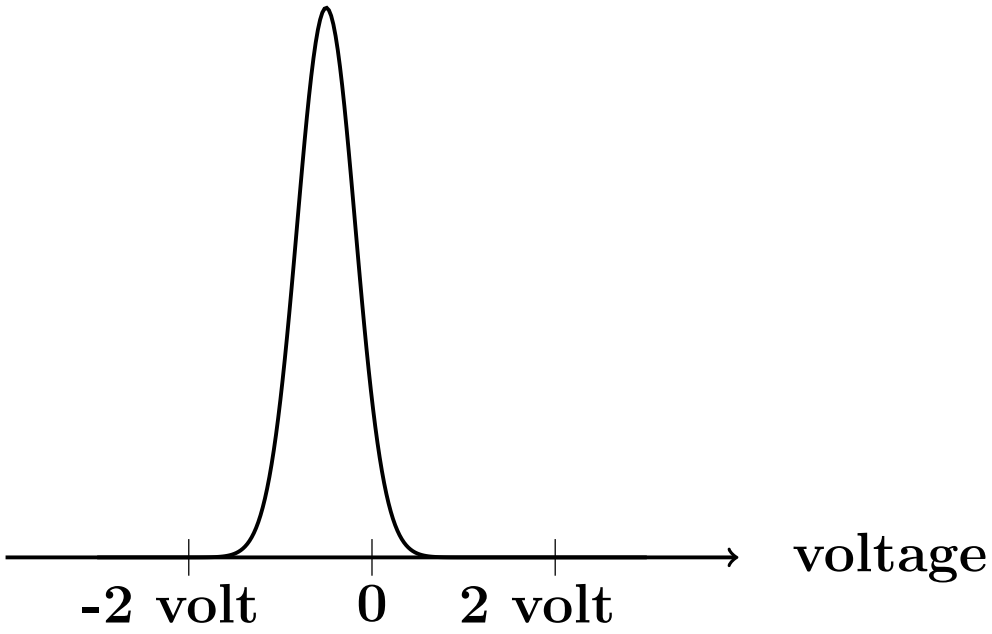

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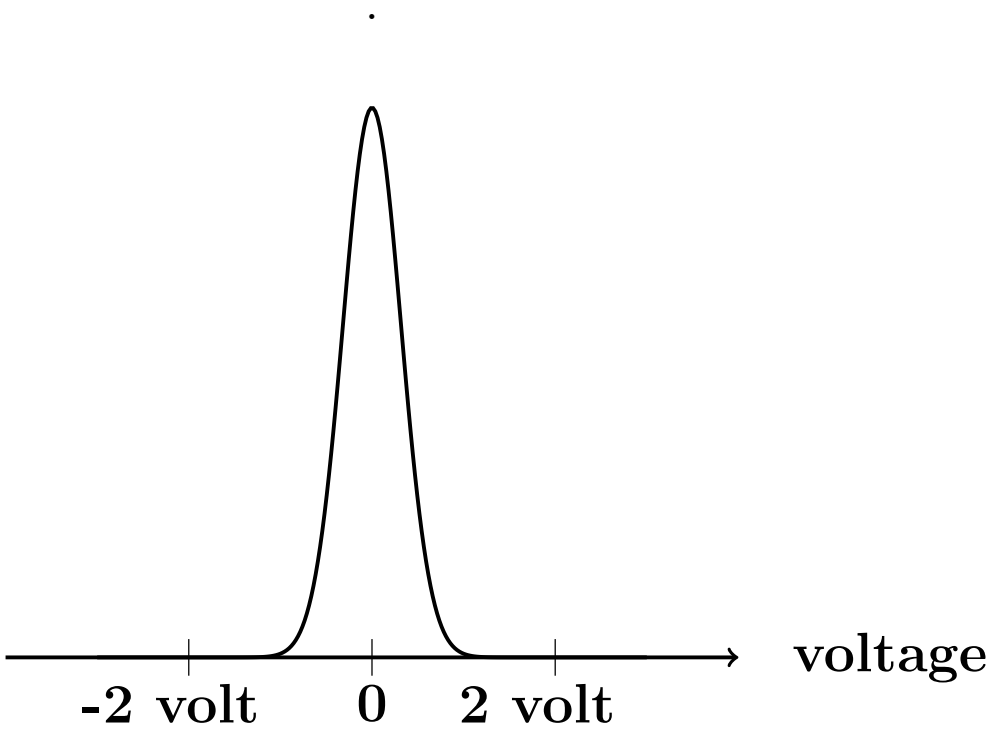

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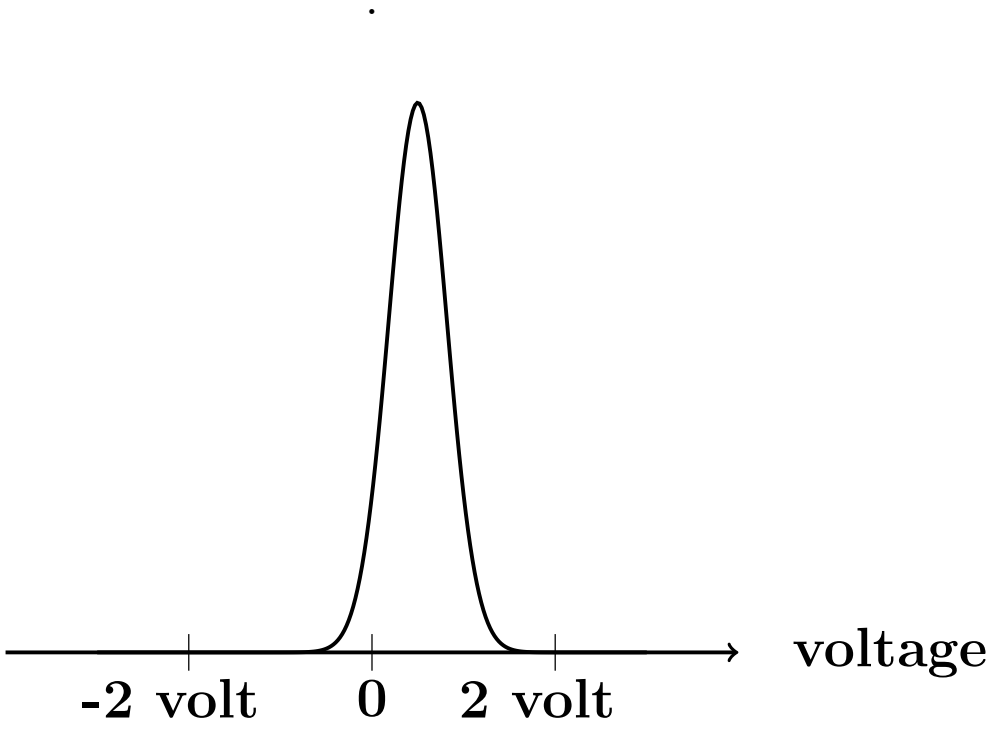

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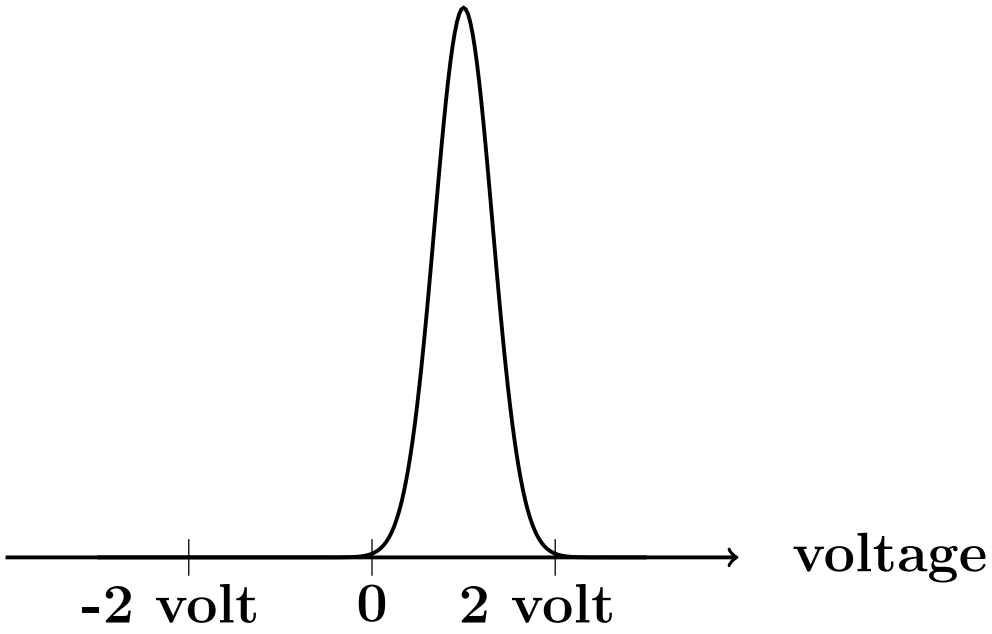

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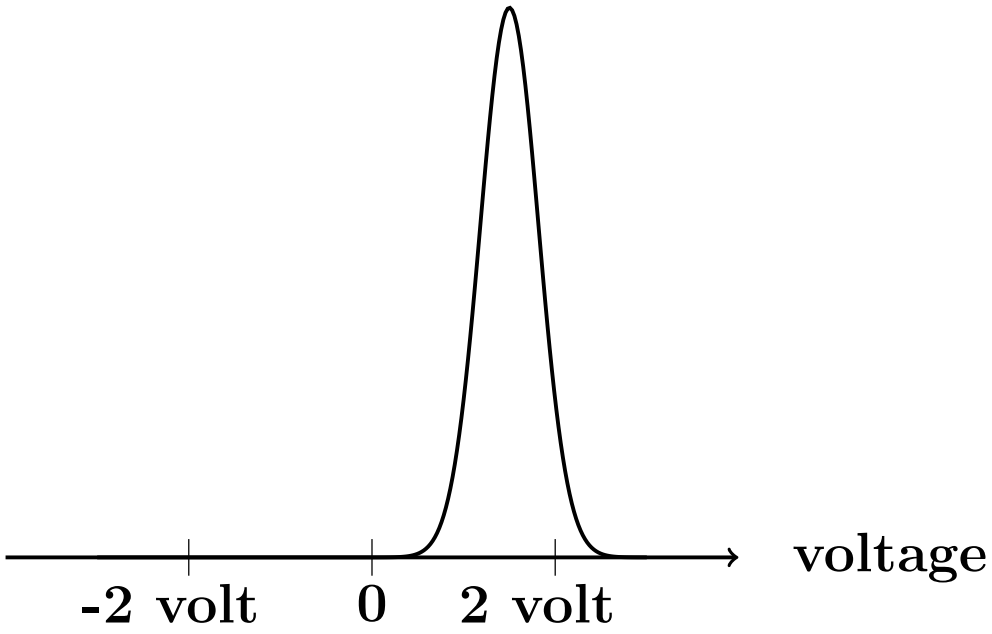

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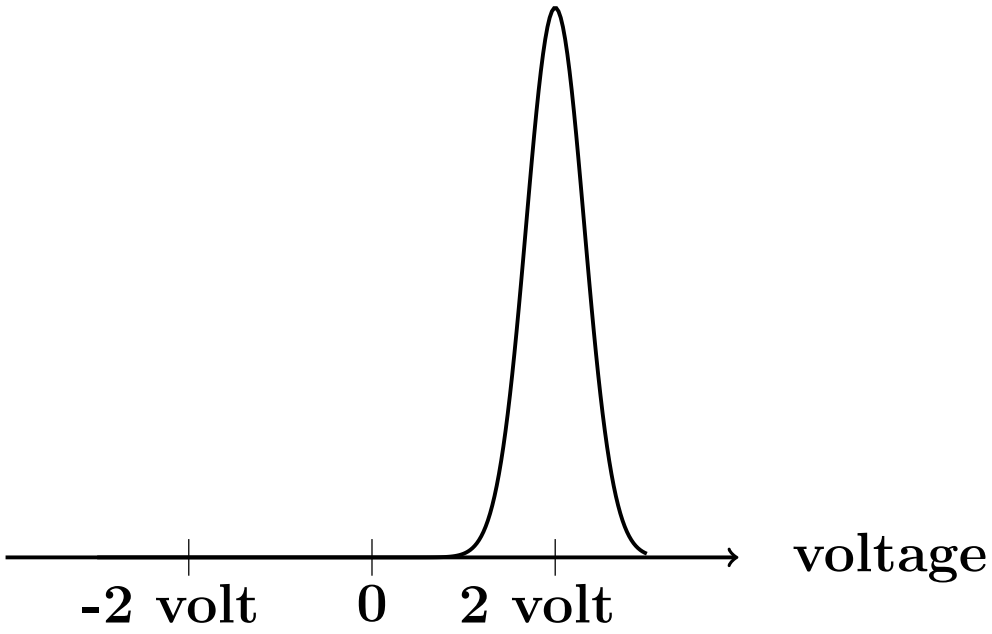
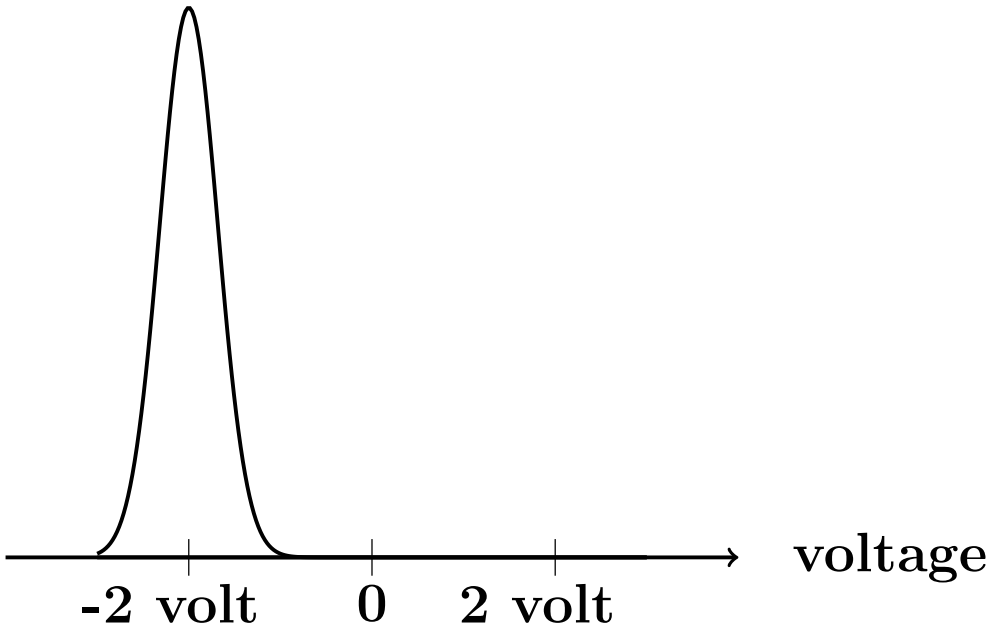


Probability distribution during quantum transition from logic 0 to logic 1



Probability distribution during quantum transition from logic 0 to logic 1

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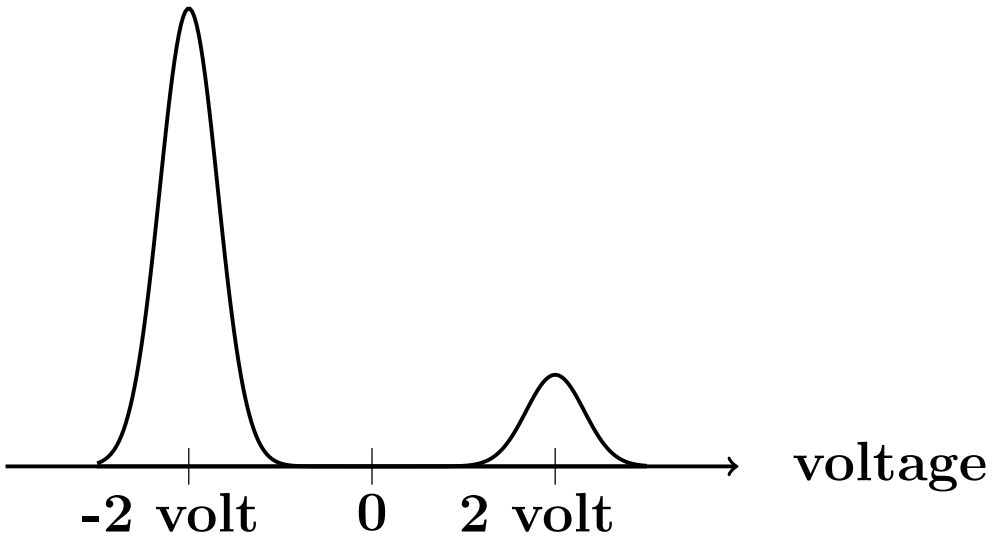

Probability distribution during quantum transition from logic 0 to logic 1

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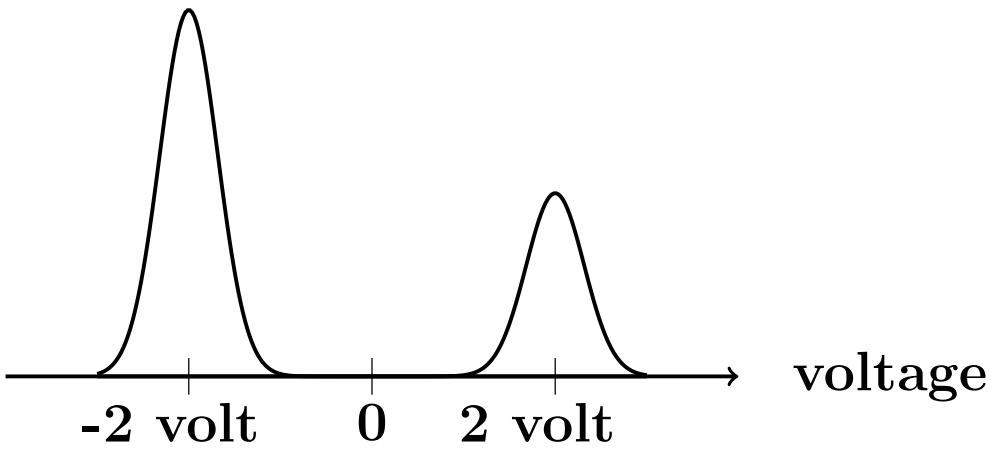

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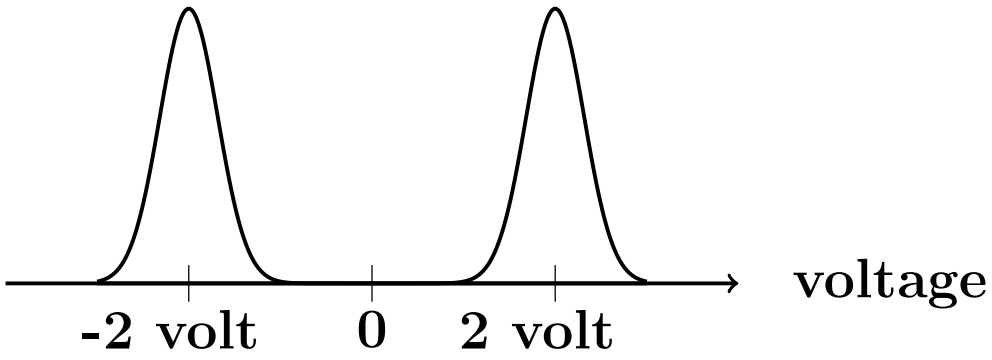

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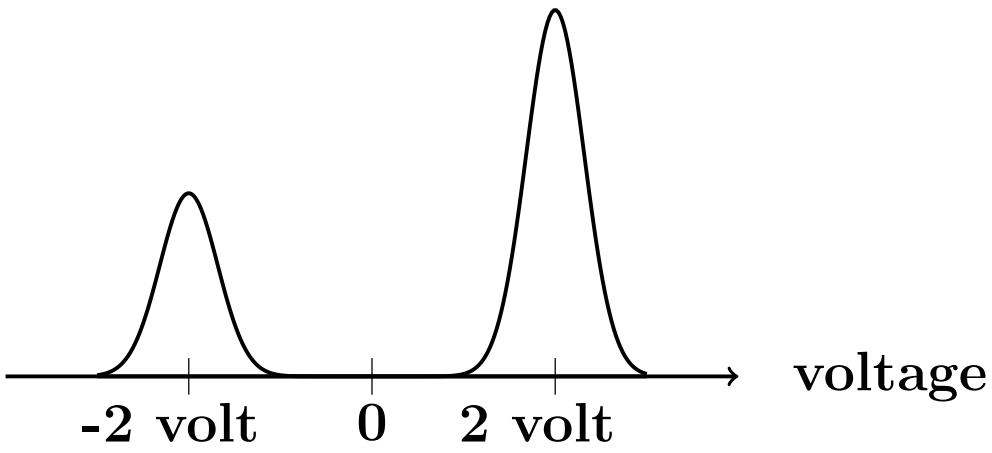
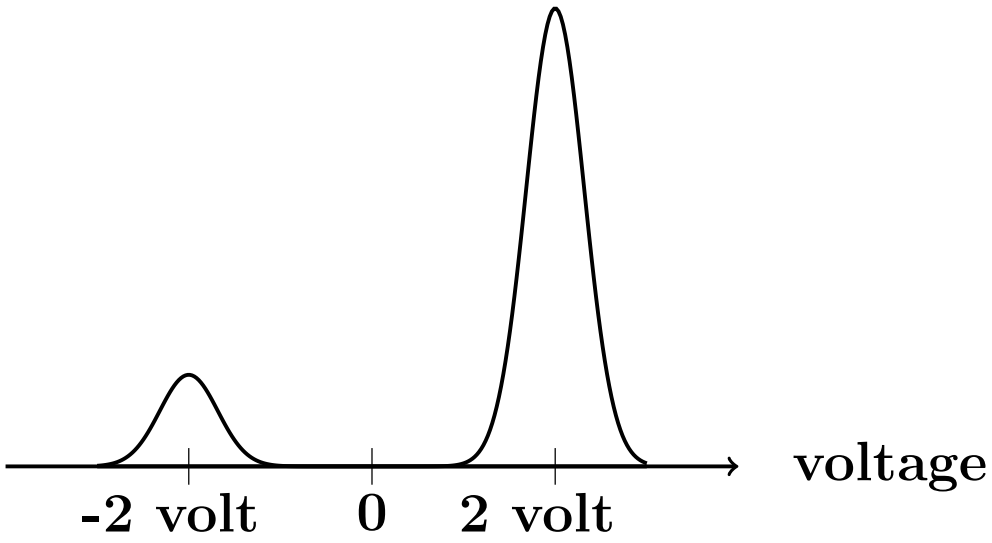


Probability distribution during quantum transition from logic 0 to logic 1



Probability distribution during quantum transition from logic 0 to logic 1