SINGLE-ELECTRON DETECTION AND MEMORY USING A SINGLE CARBON NANOTUBE DEFECT

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A single scattering center in a p-type semiconducting carbon nanotube is used as a single-electron sensitive electrometer with charge noise <0.1 $e/Hz^{1/2}$ at a temperature of 200 K. A single-electron memory is demonstrated using the nanotube electrometer as the readout device and a charge trap in the SiO_2 dielectric as the storage node. Controlled switching between discrete charge states corresponding to a difference of one electron at the storage node is detected by the electrometer as discrete current steps of more than 70 nA, with quantized threshold voltage shifts of ~200mV in the transistor transfer characteristics.

INTRODUCTION

In recent years, a large effort in single electronics research has been aimed at fabricating nonvolatile memories that store information in a single electronic charge at a write voltage comparable to the thermal energy at room temperature (1). To develop successfully such an ultra-low-power single electronic memory, two main technological challenges must be met; the charge trap must be small enough to avoid thermally activated charge fluctuation; and the detector must be sensitive enough to see the potential difference due to one charge at the trap site. Furthermore, these challenges should be met without significantly sacrificing current drivability to be useful in a commercial technology. A variety of single-electronic traps coupled to single-charge-sensitive electrometers based on Si (1-3), GaAs (4, 5), or Al/Al_2O_3 (6-9) nanofabrication technologies have been employed to demonstrate the feasibility of single- or few-electron memories. However, these devices performed with insufficient current drivability due to significantly reduced carrier mobility as a result of downsizing the active device regions to the nanometer scale necessary for Coulomb blockade to be effective at room temperature. Recently a charge-storage memory using a high-mobility semiconducting carbon nanotube field effect transistor (TubeFET) (10) with a SiO_2 gate dielectric as the readout was realized (11); the high-mobility of the TubeFET allows rewritable memory at the level of a few charges with current drivability far exceeding the capability of state-of-the-art silicon-based single-electron memories. Here we report on the use of a single scattering center in a TubeFET as an electrometer. The memory cell thus realized shows controllable switching between discrete charge states with a larger threshold voltage shift and current drive than the previously reported TubeFET memory. Moreover, the device exhibits a regular, well-defined series of charge states which allow quantitative analysis of the device parameters and an estimation of the size of the charge trap.

EXPERIMENTAL

The starting substrate for our device is 500-nm-thick SiO_2 thermally grown on a degenerately-doped Si wafer which serves as a gate electrode. The substrate was dipped in a solution of ferric nitrate in ethanol prepared as in (12) for 20 s followed by 5 s dip in hexane, and dried with N_2 gas. A piece of alumina substrate coated with iron/molybdenum catalyst prepared as in (13) was placed upstream from the chip to promote nanotube growth. The chip and the alumina piece were loaded into a quartz tube furnace, which was purged with Ar (700 ml/s) for 10 min at 300 K. Ar (600 ml/s) and H_2 (500 ml/s) were co-flowed while raising the furnace temperature to 1200 K. At 1200 K, the chip and the alumina piece are exposed to Ar (600 ml/s) for 1 minute before exposure to methane (3500 ml/s) for 6 minutes followed by flow of methane (1100 ml/s) for 20 minutes for nanotube growth. Ar (700 ml/s) flow is maintained while cooling the furnace to room temperature. Cr/Au alignment markers were patterned on the SiO_2 surface by electron beam lithography and lift-off. Nanotubes were located with respect to the alignment markers using atomic force microscopy (AFM). A second lithography and lift-off is used to define Cr/Au source and drain contacts to the nanotube. Low temperature transport measurements were carried out in a ^{4}He gas-flow cryostat [Desert Cryogenics]. Scanning gate microscopy (SGM) measurements were performed in a scanned probe microscope (JEOL JSPM-4210) operating in air at room temperature.

RESULTS AND DISCUSSIONS

Figure 1(a) shows the geometry of the nanotube device. A 3-μm-long semiconducting nanotube is contacted by source and drain electrodes separated by 1.85 μm. The nanotube has a diameter 3 nm as determined from the height profile of this AFM image. Electrical measurements (see below) verified that the nanotube was semiconducting. In order to investigate the local electronic structure of the nanotube, we used scanned gate microscopy (SGM). SGM maps the conductance changes in a device as a function of the position of a conducting scanned-probe tip used as a local electrostatic gate. The technique has been previously employed to study local potential modulations and scattering centers in nanotubes (14-16). Figure 1(b) shows an SGM image of the device. Here a metal-coated Si tip driven near its resonance frequency (~60 KHz) and biased at 4 V relative to the drain and gate contacts was scanned over the device at 1 μm/s while applying 100 mV to the source contact and monitoring the drain current to determine the resistance. The contrast scale in the image indicates the change in device resistance measured at the tapping frequency; dark indicates large resistance change. The nanotube appears darker than the surrounding substrate, indicating that the entire nanotube is semiconducting. One particularly dark region of the nanotube is evident, located about 1.3 μm from the left contact. A line trace of the SGM image along the nanotube (figure 1(c)) shows a sharp peak at this spot with a FWHM of ~30 nm and a height approximately five times greater than elsewhere along the nanotube. The spot has no corresponding topographic feature in the AFM image. We interpret this spot as due to a single atomic-scale defect in the nanotube; similar spots of large gate-voltage dependence have been observed in metallic nanotubes (16) and were similarly interpreted.

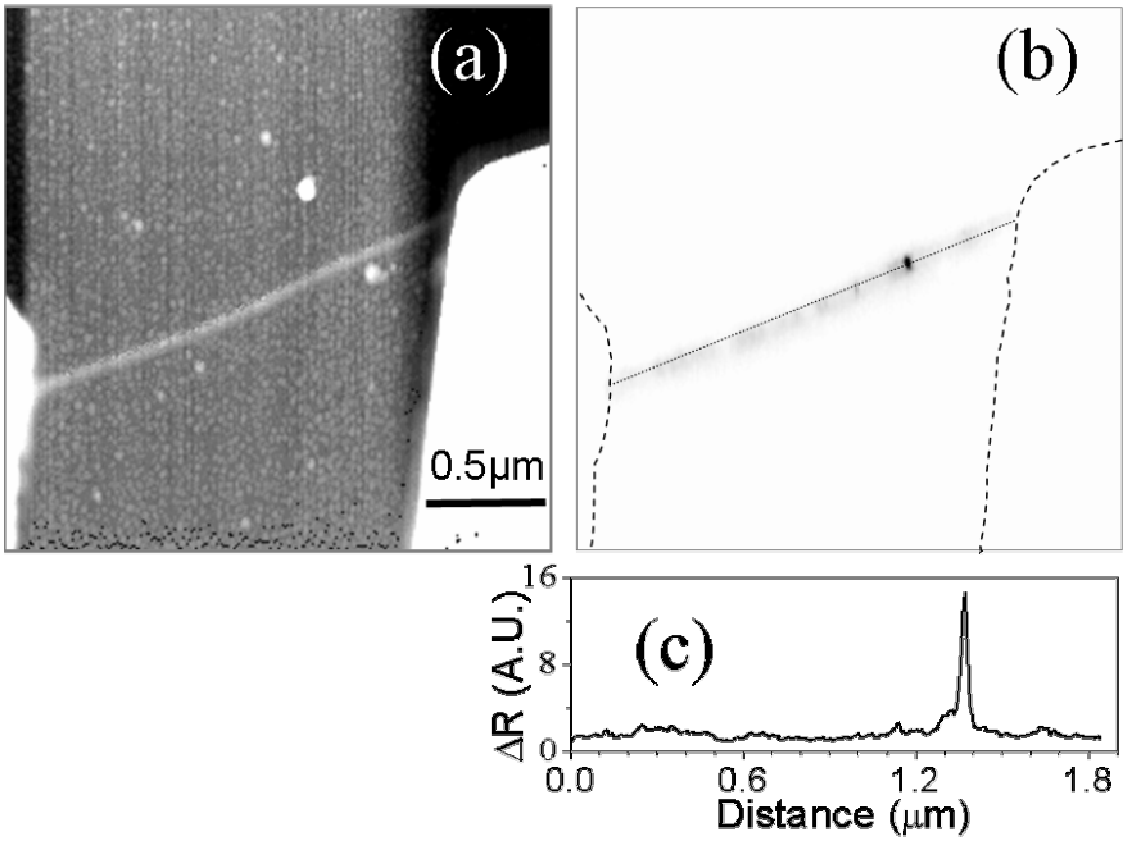

Figure 1. (a) Atomic force micrograph (AFM, intermittent-contact mode) of the nanotube device in this study. The white blocks to the left and right are the source and drain electrodes. The narrow horizontal gray line is the nanotube (length 1.85 μm, diameter 3 nm). (b) Scanned gate microscopy (SGM) image acquired simultaneously to (a). The image shows the change in resistance of the device in grayscale (darker is larger resistance change). The tip was biased at 4 V relative to the drain electrode, and 100 mV was applied to the source electrode. The change in resistance was monitored at ~60 kHz, the drive frequency of the AFM cantilever. (c) Line trace of the SGM image along the dotted line in (b).

We now turn to the electrical transport characteristics of the device. Figure 2(a) presents the drain-current (I_D) versus gate voltage (V_G) characteristics of the device measured at 100 K. The overall behavior shows a trend towards lower current (lower conductance) at higher V_G; this is indicative of semiconducting behavior for this nanotube (17,18). It is notable that I_D versus V_G is multiple-valued; several discrete I_D-V_G curves are seen, with hysteretic switching between the curves occurring at specific ranges of gate voltage. We interpret the multiple I_D-V_G curves and hysteresis loops observed in Figure 2(a) as due to single-electron charging of a trap site near the nanotube channel. This behavior has been observed previously in a nanotube transistor (11), but with somewhat smaller and more irregular shifts in V_G between I_D-V_G curves. Since the gate voltage dependence of the conductance of the device is dominated by a single defect as observed in Figures 1(b) and 1(c), we postulate that the trap site is strongly coupled to this defect, and changes in the potential of this defect due to charges at the trap site result in the

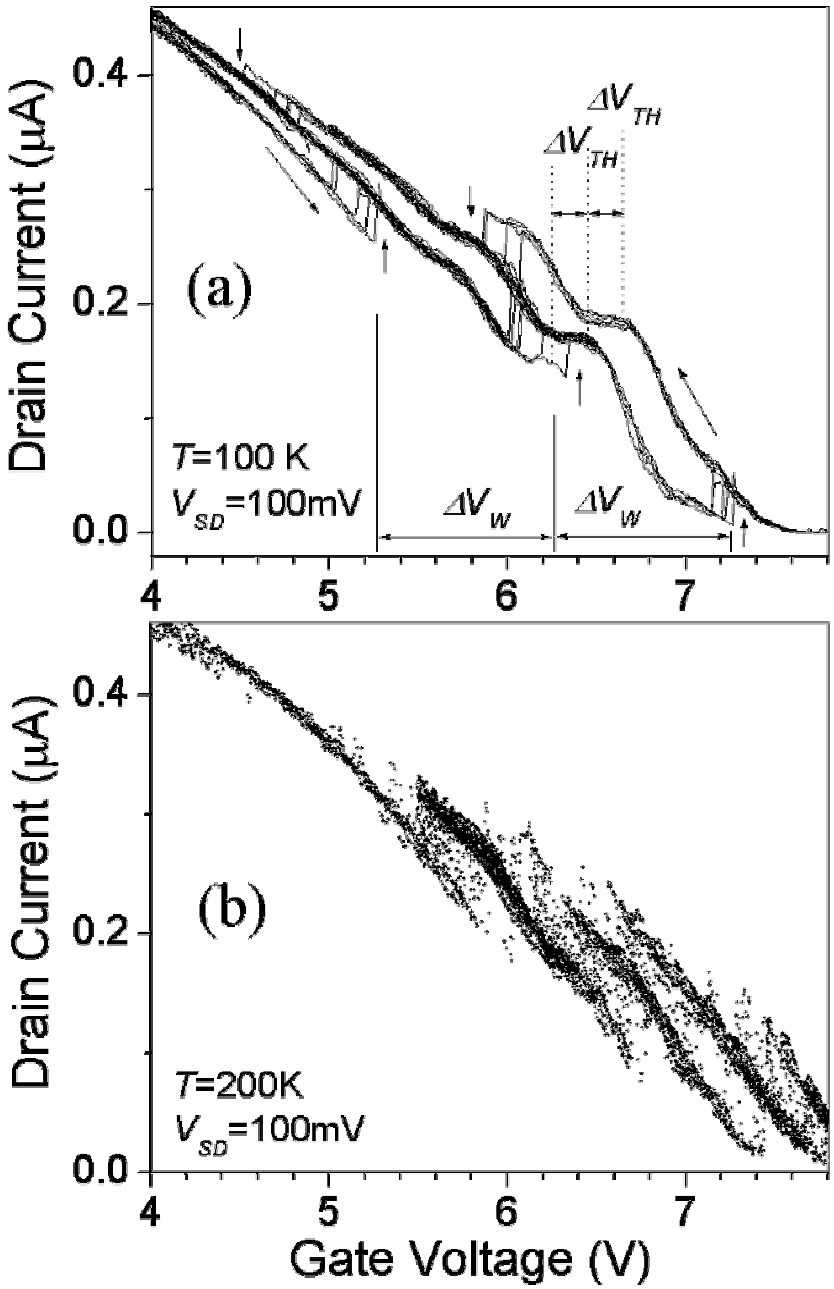

Figure 2. (a) Drain current I_D as a function of gate voltage V_G for the nanotube device at a temperature of 100 K. Four discrete I_D - V_G curves are seen, with no intermediate values of I_D. Three hysteresis loops are evident in the figure. Several sweeps back and forth over V_G ranges 5-7.8 V, 4-6.5 V, and 3-6 V are shown; these ranges were chosen to sweep out the three hysteresis loops. Arrows indicate the sweep directions. ΔV_{th} indicates the shift in V_G between the I_D - V_G curves; $\Delta V_{th} \approx 200$ mV. ΔV_w indicates the shift in V_G between the jumps between I_D - V_G curves; $\Delta V_w \approx 1$ V. (b) I_D versus V_G at a temperature of 200 K plotted as scattered points. Random switching between curves was observed as V_G was swept back and forth between 4 and 8 V.

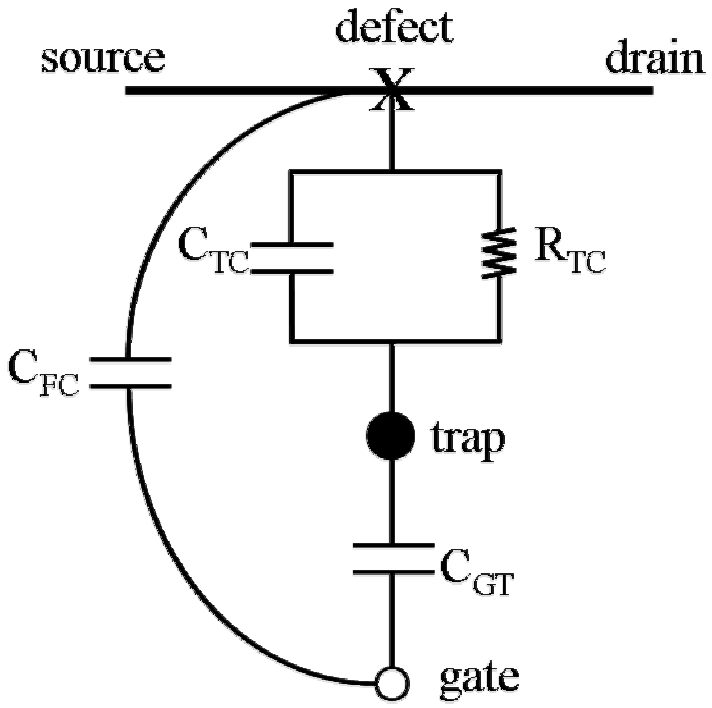

Figure 3. Schematic of the device. Source and drain denote the contacts to the nanotube channel, the defect is the spot of high gate-voltage dependence on the nanotube observed in the scanned gate microscopy image in figure 1(a), the gate is the conducting silicon substrate, and the trap is a charge trap located presumably at the surface or in the bulk of the SiO_2 dielectric.

various curves seen in Figure 2(a). Because the device behavior is dominated by a single charge trap and a single defect region acting as the electrometer, a regular series of I_D-V_G curves is seen corresponding to differences in charge at the trap of one electron.

Figure 3 shows a probable schematic of our device. The charge trap (either at the SiO_2 surface or in the SiO_2 bulk) is coupled capacitively to the defect in the nanotube channel through a capacitance C_{TC}, and to the gate through a capacitance C_{GT}. There is also in additional capacitance between the gate and channel, C_{FC}. In addition, a non-linear resistor must be present between the nanotube channel and the charge trap to allow charging and discharging of the defect. Such a device structure has been considered in detail in (1), where it was shown that this structure forms the basis of a single electron memory. The I_D-V_G characteristics of a transistor coupled to a charge trap in this way will show discrete curves, separated in gate voltage by an amount

$$\Delta V_{th} = \frac{eC_{TC}}{(C_{TC} + C_{GC})C_{GC}} \qquad [1]$$

where e is the electronic charge and C_{GC} is the total gate capacitance given by

$$C_{GC} = C_{FC} + \frac{C_{TC}C_{GT}}{C_{TC} + C_{GT}} \quad [2]$$

Periodic switching events will occur between curves with a spacing

$$\Delta V_w = \frac{e}{C_{GT}} \quad [3]$$

and the hysteresis width (the distance in gate voltage between the switching events between two charge states of the trap when increasing gate voltage and decreasing gate voltage) is determined by the nonlinear characteristics of the resistor R_{TC} between channel and charge trap (1).

For our device, we observe a threshold shift $\Delta V_{th} \approx 200$ mV, and a write voltage periodicity $\Delta V_w \approx 1.0$ V (see Figure 2(a)). These two numbers are insufficient to determine the three capacitances in Figure 3. We may estimate one of the capacitances, C_{FC}, by estimating the size of the defect region in the channel. From the SGM line trace (Figure 1(c)), the defect region is approximately 30 nm in extent (or perhaps smaller, this distance is comparable to the resolution of the image). This distance can be interpreted as the screening length in the nanotube at the defect. From Coulomb blockade measurements of other devices, we know that the gate capacitance per length of our nanotube transistors is approximately 10 aF/μm. This gives a capacitive coupling $C_{FC} \approx$ 0.30 aF between the defect region and gate. Solving for the other capacitances, we find $C_{TC} \approx 0.14$ aF and $C_{GT} \approx 0.16$ aF. The total capacitance of the charge trap $C_{TT} = C_{TC} + C_{GT} = 0.30$ aF. From this value we can make a rough estimate of the size of the charge trap. The self-capacitance of a sphere of radius r is given by $C_{self} = 4\pi\varepsilon\varepsilon_o r$, where ε_o is the permittivity of free space and ε the dielectric constant of the medium in which the sphere is embedded, ~4 for SiO_2. Setting $C_{TT} = C_{self}$ gives $r = 6.7$ Å, reasonable for a vacancy site or complex of dangling bonds in the SiO_2 dielectric.

The total capacitance of the charge trap gives a Coulomb charging energy $E_c = e^2/C_{TT} \approx 530$ meV. Coulomb blockade should be effective up to a temperature $k_B T$ of order 0.1 E_c, or approximately 600 K. Figure 2(b) shows the I_D-V_G characteristics for the device at a temperature of 200 K in the form of a scatter plot. The I_D-V_G data are observed to fall on a set of discrete curves, but random telegraph switching between the curves was observed at all gate voltages. The observation of discrete I_D-V_G curves indicates that Coulomb blockade of the charge trap is indeed still effective at 200 K, but the random telegraph switching indicates that the nonlinear resistance R_{TC} between channel and trap has become leaky at elevated temperatures, allowing the charge on the trap to fluctuate. The data in Figure 2(b) are taken at a bandwidth of 10 Hz; from the fact that the curves corresponding to single electron differences at the charge trap are well resolved, (signal to noise ratio > 3) we estimate that the nanotube defect electrometer has a sensitivity better than 0.1 $e/\mathrm{Hz}^{1/2}$ at 200 K.

We now turn to memory operation of the device. Figure 4(a) shows the drain current I_D and gate voltage V_G as a function of time at a temperature of 5 K. The drain current was read at a gate voltage of 6.75 V, and periodic pulses to 5 V or 8 V were used to switch the charge state of the trap. A current of more than 70 nA is switched with only 100 mV source-drain bias. The high and low current states are stable for at least one hour. Figure 4(b) shows an attempt at operation of the memory at 200 K. At this temperature the charge states are not stable, and random telegraph noise is observed as the charge state of the trap switches. Improvement of the resistance path R_{TC} through which the trap is charged and discharged should allow high temperature operation of the device.

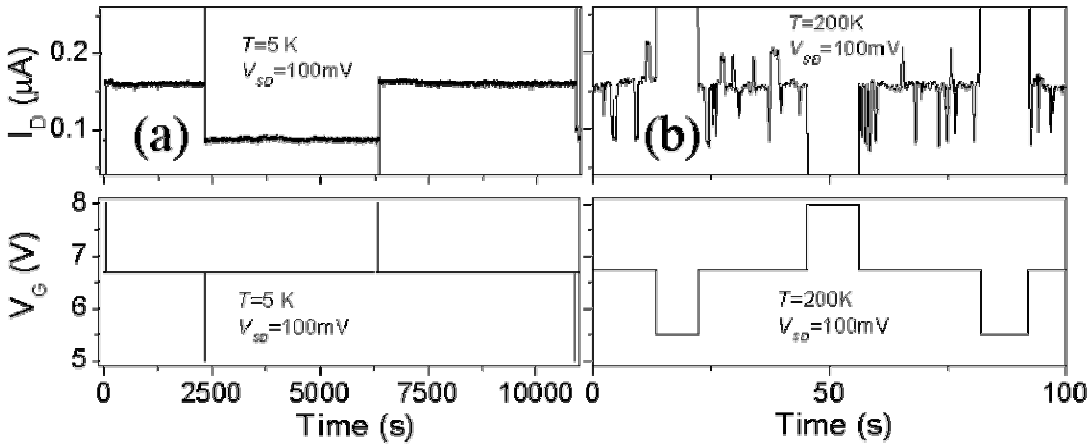

Figure 4. Memory operation of the device. (a) Reading, writing, and erasing a single electron in the charge trap at a temperature of 5 K. The upper panel shows the drain current I_D, while the lower panel shows the gate voltage V_G, as a function of time. The memory state is read at V_G = 6.75 V, and written or erased with pulses of V_G to 8 V or 5 V, respectively. The current is switched from a high state (~160 nA) to a low state (~90 nA) and back again. Each state is stable for at least 4000 seconds. (b) Attempted memory operation at 200 K. The trap charge states were unstable at this temperature, and only random telegraph switching between states is observed. Three current states (~90, 160, 210 nA) are observed at V_G = 6.75 V.

ACKNOWLEDGEMENTS

This research was supported by ARDA and the Office of Naval Research through grant N000140110995, the Director of Central Intelligence Postdoctoral Research Fellowship Program, and the National Science Foundation through grant DMR-0102950. The authors are grateful for helpful conversations with Frank D. Gac.

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