Gate-Field-Induced Schottky Barrier Lowering in a Nanotube Field-Effect Transistor

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Abstract. We propose that in nanotube field effect transistors (FETs) with small effective dielectric thickness the vertical potential drop across the nanotube diameter at finite gate bias can lower or eliminate the Schottky barrier at the electrode. This effect is demonstrated in single-walled carbon nanotube FETs fabricated on top of ultra-high-κ dielectric constant $SrTiO_3$/Si substrates. These FETs show transconductances normalized by channel width of 8900 S/m, one of the highest values to date. This transconductance cannot be explained within the conventional FET or Schottky-barrier models.

INTRODUCTION

The possibility of using semiconducting single-walled carbon nanotubes (CNT) as a replacement for, or complement to, silicon within a field effect transistor (FET) architecture has led to an intense research effort into both the NTs themselves and the NTs interfaced with technologically relevant materials. The intrinsic nanometer scale and pristine quality of the carbon lattice in SWNTs initially inspired great hope for a semiconducting, ballistic, easily manufacturable nanoscale material for use in FETs [1]. However, the Schottky barrier (SB) at the CNT-metal interface limited the improved performance with traditional vertical scaling (thinner dielectrics and higher dielectric constants) [2]. Subsequent efforts focused on either avoiding the SBs through engineering solutions or by achieving Ohmic contact with high work function metals and large diameter, smaller band gap SWNTs [3-5]. Continuing this research effort, we report here the integration of high-κ $SrTiO_3$ on Si substrates (STO/Si) with NT-FETs. The high transconductance per channel width (8900 μS/μm), limited number of lithography steps, and use of small-diameter NTs indicates an alternate avenue for high-performance CNT-FET fabrication. We explain the scaling of the transconductance as the emergence of a new vertical length regime within the Schottky barrier model, which causes a gate-induced Ohmic contact.

DEVICE FABRICATION

Our starting substrates were epitaxial STO/Si (κ ≈ 175). Details on the growth and characterization of this STO/Si have been reported elsewhere [6]. CNTs were grown

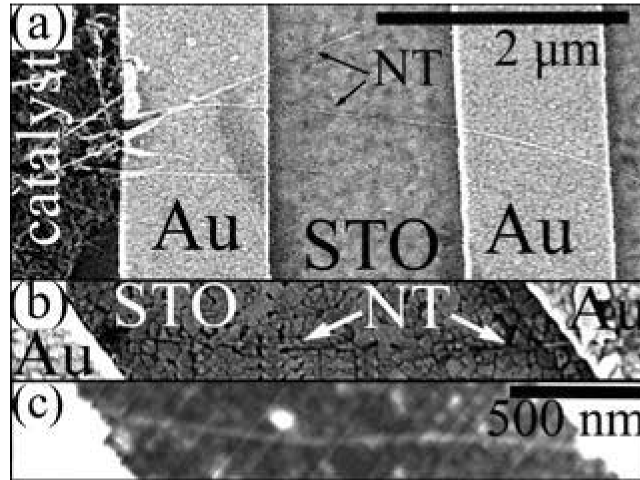

FIGURE 1. Images of CNT-FETs grown on $SrTiO_3$ (STO) substrates by chemical vapor deposition. Part (a) shows patterned catalyst (left) on STO, as well as several nanotubes extending from the catalyst island. One nanotube has been contacted by two Cr/Au electrodes. (b) Field-emission scanning electron micrograph of a semiconducting nanotube on STO bridging two Cr/Au contacts with 1.8 um separation. (c) AFM image of the nanotube in (b), giving a NT diameter of 1 nm.

by chemical vapor deposition (CVD), adapting from procedures for synthesis of CNTs on SiO_2. The resulting CNT-FETs are shown in Figure 1. Parts (a) and (b) show scanning electron microscope (SEM) images, employing a technique originally developed with SiO_2/Si substrates [7]. Part (c) illustrates a typical atomic force micrograph, used to determine NT diameter (1 nm in (c) and for measurements in this paper). Briefly, an alumina-supported Fe/Mo catalyst was patterned in islands on the substrate by electron-beam lithography. CVD synthesis was carried out in a 1 in. diameter tube furnace for 11 min at 900 ºC using a methane/hydrogen co-flow. To ensure the STO/Si remained intact after growth and to verify the STO thickness, we performed transmission electron microscopy (TEM) and electron diffraction, shown elsewhere [8]. Transport results are shown in Fig. 2 below, with discussion following.

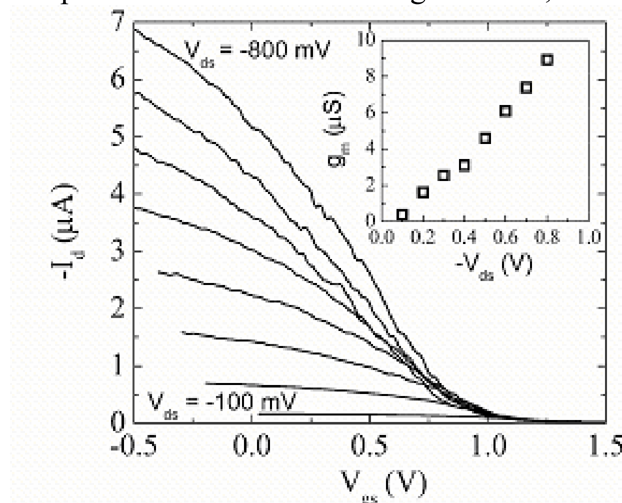

FIGURE 2. Drain current (I_d) vs. gate voltage (V_{gs}) at different bias voltages (V_{ds}) for a 1 nm CNT-FET. Inset shows peak transconductance (g_m) vs. V_{ds} through numerical differentiation of the curves in the main graph. The highest g_m at 800 mV bias is one of the highest to date.

RESULTS AND DISCUSSION

We have measured the electrical properties of CNT-FETs on STO using the Si substrate as a global back gate. Figure 2 shows the behavior of a typical device with the drain current, I_d, changing as a function of gate voltage, V_{gs}, for different bias voltages, V_{ds}. The inset shows peak transconductances, $g_m = dI_d/dV_{gs}$, determined by numerically differentiating the curves in the main graph, versus V_{gs}. The peak transconductance at 800 mV is 8.9 µS. To compare to other CNT-FETs, we divided by the channel width, the NT diameter, to obtain 8,900 µS/µm, one of the highest values to date (see Table 1). We also note that this value is most likely not in the saturation regime, and thus g_m may go even higher with increasing V_{ds}. In comparing this device with others, we first attempted to model its behavior within the 1D diffusive FET model in which the transconductance in the saturation region is given by $g_m \approx \mu c_g V_{ds}/L$, where μ is mobility, c_g is gate capacitance per length and L is channel length. Thus for a given material system (given μ) the transconductance can be increased through increasing c_g or V_{ds}, or decreasing L. In practice, however, the product $\mu V_d/L$ is expected to saturate in v_s, the saturation carrier velocity, and the maximum transconductance is $g_{m,\max} = c_g v_s$. Thus increasing c_g becomes the goal for obtaining higher transconductance. In comparing our g_m (or g_m/d) with other published values of g_m, we see that it is 10-15 times larger than other values while the (quantum capacitance-limited) total gate capacitance, c_g, is only 3-5 times larger. This is not surprising as other workers have shown that SBs at the NT-metal interface greatly influence CNT-FET performance [9]. In Ref. 9, the vertical scaling of the SB effect on CNT-FET is investigated, and it is shown that $g_m \sim t^{-1/2}$, where t is the oxide thickness, and this scaling occurs *independent of dielectric constant*. Again comparing our results with Refs. 1 and 2 in Table 1, we see that the oxide thickness of our CNT-FETs is greater than or equal to the others while g_m is 10-15 times larger, an inadequate explanation of the behavior of our CNT-FETs. A third possible explanation of the high transconductance is Ohmic contact at the NT-metal interface, as shown in Ref. 4, but small diameter ($d < 2$ nm) NTs and unannealed Cr/Au contacts are shown to make poor/non-Ohmic contacts in Ref. 4 and Ref. 10 respectively. So we consider this possibility unlikely.

TABLE 1. Device parameters for CNT-FETs in this and other works.

Author	Dielectric (κ)	t (nm)	d (nm)	c_g (pF/cm)	g_m (µS)	V_{ds} (V)	g_m/d (µS/µm)
Bachtold (Ref. 1)	Al_2O_3 (5)	2-5	1	0.7-1.0	0.3	-1.3	300
Appenzeller (Ref. 2)	HfO_2 (11)	20	1-2	1.1	0.6	-1.5	300-600
This work	$SrTiO_3$ (175)	20	1.0	3.4	8.9	-0.8	8900
Javey* (Ref. 3)	ZrO_2 (25)	8	2	2.3	12	-1.2	6000
Nihey* (Ref. 3)	TiO_2 (40-90)	2-3	1.5	3.0	8.7	-1	5800
Javey*† (Ref. 4)	HfO_2 (20)	8	2.3	1.7	20	-0.5	10000
Rosenblatt‡ (Ref. 5)	Electrolyte (80)	~1	3	3.8	20	-0.8	6700

The columns display the dielectric material and dielectric constant κ, dielectric thickness t, nanotube diameter d, total gate capacitance c_g, transconductance g_m, source-drain bias V_{ds} and transconductance per width, g_m/d. The symbol * denotes local top gating, † Ohmic contacts, and ‡ electrolytic gating.

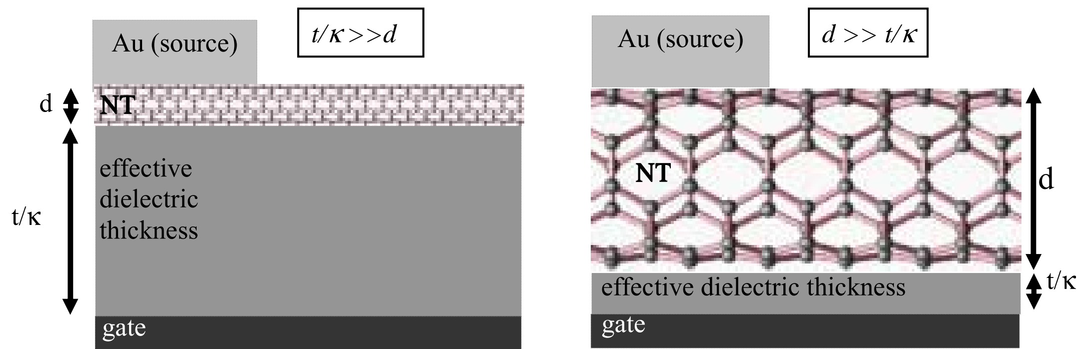

FIGURE 3. Visual model of different vertical length regimes within the Schottky barrier model. The left image shows a picture of the length regime described in Ref. 10, while the right image describes the length regime in this work.

Another possibility is that vertical scaling has a more pronounced effect on the Schottky barriers. The model of Ref. 9 may be inadequate for ignoring charge in the nanotube channel [11] and for treating the NT as infinitely thin. We expect the electric field at the contacts will be substantially modified when the effective thickness of the dielectric $t' = t/\kappa$ becomes significantly less than the CNT diameter d (where $\kappa_{NT} \sim 1$ [12]). In our devices, $t'/d \approx 0.1$ is significantly less than the values of $t'/d \approx 0.4$-1 and 1-2 in Refs. 1 and 2 respectively (see Fig. 3). For $t'/d << 1$, the potential drop *across* the CNT diameter becomes a large fraction of V_{gs}. When the potential drop across the radius of the nanotube is equal to the SB height, population of the valence band with carriers should become energetically favorable, allowing Ohmic contact with the channel. Stated another way, at moderate V_{gs}, the potential of the NT relative to the electrode can be greater than the SB height, eliminating the barrier. In our devices, this would occur at a V_{gs} of a few hundred mV from threshold. This model also offers an alternate explanation for the observation of high transconductances (even in small diameter CNTs) in FETs with an electrolyte dielectric ($t'/d \approx 0.01$) [5].

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