CMS Internal Note 99-xxxxx
January 24, 2000
Version 2

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Conceptual Design
CMS HCAL Upper Level Readout System

D. Baden, R. Bard, J. Giganti
University of Maryland

J. Elias
Fermi National Accelerator Laboratory

E. Hazen, E. Machado, L. Sulak
Boston University

Abstract

This document serves as a Design Report for the HCAL upper level readout, defined as that set of electronics and functions that receive the HCAL QIE fiber output in preparation for Level 1, Level 2, and DAQ processing. This includes all readout cards, trigger primitive processing, formatting, and delivery to the (and including) the HCAL DDU.

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1 Introduction

This document presents the current conceptual design of the CMS Hadron Calorimeter (HCAL) upper level readout system. The upper level readout system is defined as everything between the optical fibers carrying the HCAL data from the detector, and the input to the L2/L3 processor Farm.

2 Overall System Design

The overall system design and its context within CMS HCAL and Trigger is shown in figure 1. Parameters are as in table 1. The full readout system consists of 24 VME crates. Each crate will be responsible for receiving HCAL data, maintaining the 40MHz pipeline, maintaining synchronization via the TTC, and preparing and transmitting the data for both Level 1 and Level 2/DAQ. To do this, the HCAL readout crate will contain:

- HTR – **H**CAL **R**eadout and **T**rigger cards: these cards are the workhorse for receiving and processing raw data for the Level 1 trigger, as well as perparation for Level 1.
- DCC – **D**ata **C**oncentrator **C**card: this card receives Level 2 data from each HTR card in the crate in preparation for transmission to Level 2 and the CMS DAQ network.
- HRC – **HC**AL **R**eadout **C**ontrol card: this card is responsible for fast and slow monitoring, as well as ancillary trigger control distribution and whatever functionality is not in the HTR and DDC card. This card will have an onboard CPU.

Each crate will consist of 18 HTR cards, 1 DCC, and 1 HRC card, and will service a single Device Dependent Unit (DDU) for Level 2/DAQ feeding. At this time, it is not clear whether the DDU is to be part of the DCC card itself. The optical fibers supplying the readout crates are not included in the system. The trigger links, however, are included, and possibly the HCAL DDU as well although this has not been entirely settled as of this time. Buffer sizes and transmission requirements will all be based around an expected average Level 1 accept rate (L1A) of 100kHz. The Level 2 accept rate is irrelevant for these considerations. Crates will reside in a room near the detector, but below the surface.

HCAL readout crates	24
DCC cards per crate	1
HRC cards per crate	1
HTR cards per crate	18
Input fibers per HTR	16
HCAL channels per fiber	2
HCAL channels per HTR	32
HCAL channels per crate	576
TOTAL HCAL channels	13,824
TOTAL HTR cards	432
TOTAL DCC cards	24

Table 1: HCAL upper level readout system parameters.

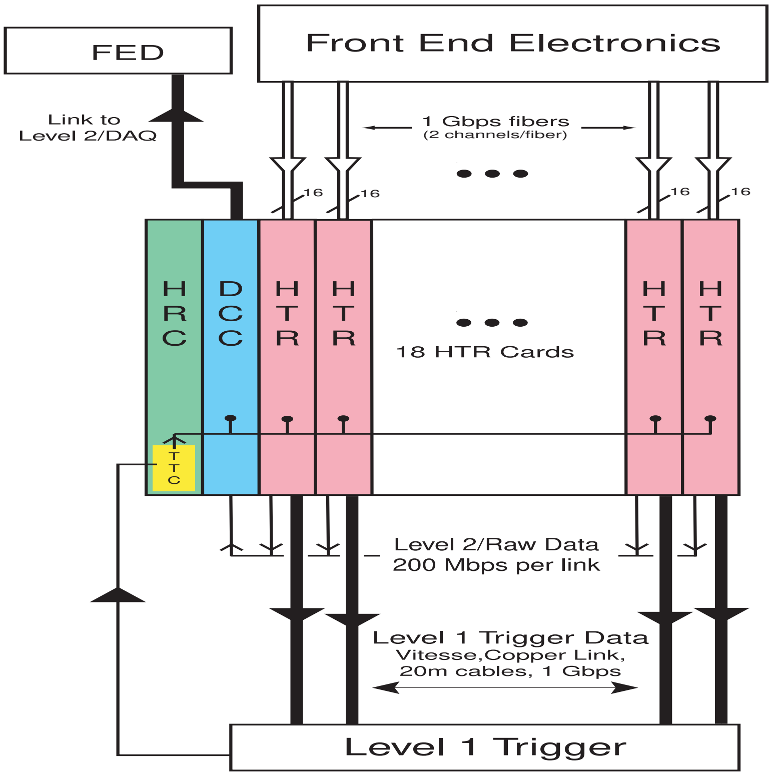

Figure 1: HCAL Readout and Trigger Crate.

3 Upper Level Readout Crate

The readout crate is mechanically a 9U x 400 mm VME crate. The P3 area is completely user definable, and will be used by HTR cards (see section 4) for transmission of trigger primitive data to Level 1 (see secton 4.2), possibly via auxiliary backplane cards but also possibly via direct connectors, eliminating any P3 backplane and associated auxiliary cards. The latter approach is seen as a cost savings. We anticipate that we will need the middle row of P2 (for VME 32) for calibration and monitoring I/O, involving the HRC card (see section 5).

HCAL data arrives at each crate via optical fiber links which delivers data at approximately 1 Gbps using the HP G-Links protocol. Each fiber will deliver 2 channels worth of data. As described in section 2, there will be a total of 18 HTR cards per VME crate, and each HTR card is anticipated to service 16 fiber inputs, bringing the total number of fibers per crate to 288, or 576 HCAL channels. Once arrived, the data is transformed, buffered, and pipelined in the HTR card. While in the pipeline, data is prepared (Level 1 "trigger primitives" are constructed) and transmitted to the Level 1 framework over copper cables. These trigger primitive cables will carry approximately 2 "trigger towers" per cable, with each trigger tower constituting the signal in both the front and back section of an HCAL physical tower. This results in 8 cables per HTR card, or 144 per crate. The maximum average L1 accept rate is required to be approximately 100kHz. If the L1 trigger passes the event, the data stored in the pipeline buffers is collected, processed and transmitted to the DCC for concentration over simple channel-link copper cables, one per HTR card, where it waits until it can be transferred to the DAQ system via DCC input cards. The DCC will hold approximately 1000 events in its internal buffers. The HRC card serves as the interface in the crates for both slow and fast monitoring, as well as providing a home for a TTC receiver (TTCRx). TTC signals will be delivered by the HRC card to the 18 HTR cards in the crate, insuring synchronization.

4 The HTR Card

In this section we discuss the HTR card, which consist of an input section for raw data receiving, a Level 1 Path containing the Level 1 preparation and transmission capaibility to the Level 1 framework, and a Level 2/DAQ Path consisting of the pipeline storage and Level 1 accept buffering used for transmission to the DCC. The HTR design takes advantage of the current (and projected) availability of large affordable FPGA chips with $\sim 10^6$ gates and $\sim 10^3$ I/O pins. This design (as opposed to having separate cards for the separate receiving and trigger functions) allows a merging of the readout and trigger preprocessing functionality into a single card, decreasing the engineering and production costs (fewer different cards) and allowing for fewer channels per card (more cards with readout capability).

4.1 Input Section

The HCAL calorimeter signals are digitized at each crossing (40 MHz). Each HCAL QIE channel will produce a 7-bit number per crossing as a measure of the energy in the HCAL element. The digital 7-bit value is a variant floating point format, consisting of 2 bits of scale (exponent) and 5-bits of ADC digitization (mantissa). Since there are 4 capacitors per QIE output, there will be an additional 2 "CAP" bits transmitted with the QIE digital number. The CAP bit will be used to correct for the variation in each sample-and-hold capacitor. Transmission will be via fiber optics using the HP G-Links protocol running in encoded mode with 20 bit frames. Each frame will consist of the data from 2 QIE channels (2x7=14 bits) plus the 2 CAP bits for a total of 16 data bits per frame. The rate of transmission will be at 40 Mframes/sec for an total data transmission bandwidth of approximately 700Mbit/sec[7].

The fibers which deliver data to the HTR cards will plug into the front panel. This scheme alleviates engineering R&D necessary for successful input over the P3 backplane, and takes advantage of the G-links built-in receiving and deserializing capability. As shown in figure 4.1, the receiver section of the HTR card will add a "frame bit" which will tag transmission errors. Synchronization errors in the cap bit will be flagged and transmitted during those buckets that come in the orbit gap, in the form of an error code[7]. A PLD will receive the 16 bits of data along with the frame bit, and transmit simultaneously to the Level 1 and Level 2 paths for processing. Note that the PLD will have the TTC timing information available. Figure 2 shows a schematic overview of the HTR card.

4.2 Level 1 Path

The L1 tap needs to be processed and summed with its other depth segments for that eta-phi tower before being sent to the L1 trigger. The HCAL signals are collected over a period of 5 crossings. The first two are for baseline subtraction, the last three are the time it takes to collect the energy. The tapped L1 signals must be processed to giver the energy in the single beam crossing which created the energy. The MCM contains a simple processor for this purpose. However, we should develop an algorithm for implementation in a gate array as an alternative should we not use the MCM. The summing is done by a combination of the readout card and trigger card. For the barrel, there are only two depth segments for each tower. This sum is performed on the readout card. For the endcap calorimeters there can 2,3 or 4 segments which need to be added. No more then two are done on the readout card, further summing is done by the trigger cards. The forward calorimeter is even more complex. After summing, the 10

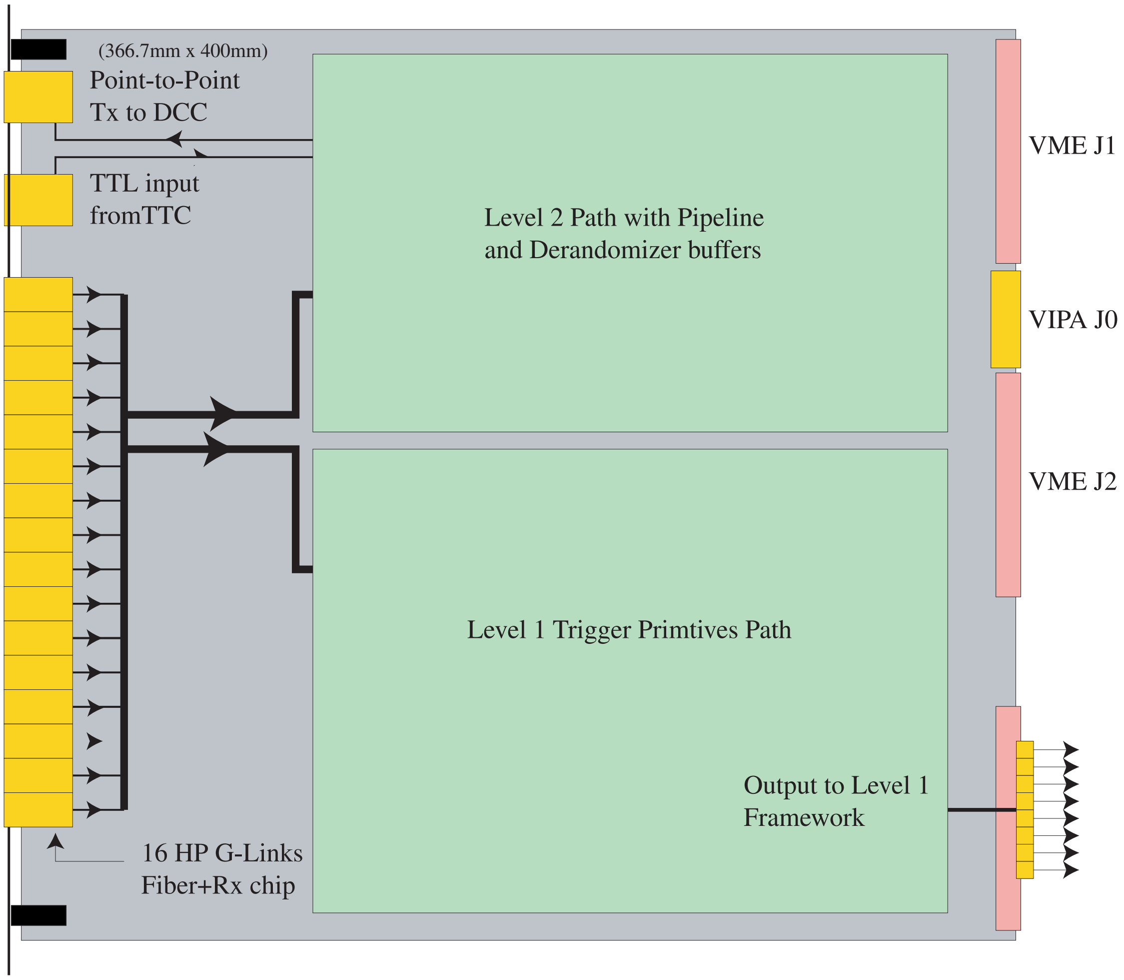

Figure 2: **HTR card layout**

bits with least count of .5 GeV are picked out of the 16 and sent to the adjacent trigger card by parallel connection across the front panel.

The Level 1 Path is fully pipelined with no buffering. **(is it here that we would use the error bits to zero the energy before summing? after summing?)** As shown in figure 4, channels which correspond to the two HCAL depths in a single HCAL tower will be added together into a 17-bit data word and passed through a Level 1 "filter" which will determine what energy to be associated with what beam crossing, producing a 16-bit word. The filter will implement a scheme involving the energy in five consecutive buckets. The most likely scheme will involve adding the energy in the 5 towers A, B, C, D, and E with the weights such that the output will be given by

$$\text{Output} = 1.0 \cdot (A + B + C) - 1.5 \cdot (D + E),$$

thus integrating over the three buckets which had real energy, subtracting any common baseline. We plan to implement this filter using an FPGA, since these weights involve only factors of 2. **(but what about the negative sign?)** The resultant 16 bits of data is then

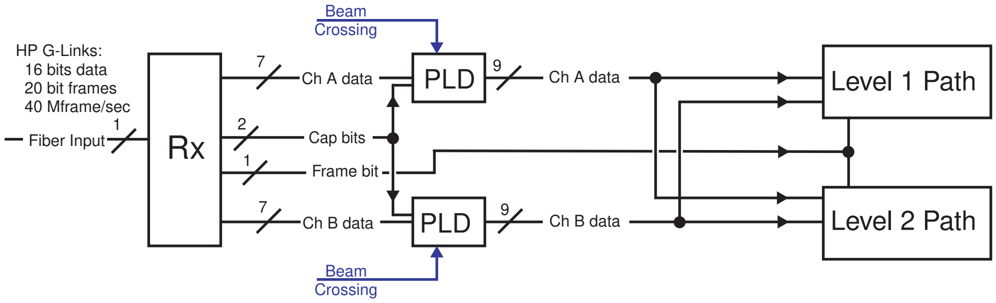

Figure 3: HTR input section.

assigned to a particular crossing (maintaining the pipeline). A “muon bit”, the result of a window calculation for the presence of a muon, is then produced and added to the data as a “feature bit”. The 16 bit HCAL tower energy is then subject to a truncation and overflow calculation, eliminating 6 bits, and then sent through a non-linear transformation further reducing the tower energy to 8 bits. **(hey guys, is this energy or transverse energy???)** Along with the feature bit, these 9 bits are combined with 9 bits of data from another tower and merged into a 24 bit Level 1 format for transmission.

As detailed in table 2, the 24 bits of Level 1 data will include 9 bits each from 2 towers, plus 5 bits of Hamming code for error recovery, plus an addition bit signifying the abort gap. **(i forget why we need to have an abort gap bit? is it so that we can use this for calibration data?**

Purpose	Bits
Tower 1 energy	8
Tower 1 muon flag	1
Tower 2 energy	8
Tower 2 muon flag	1
Abort gap flag	1
Hamming bits	5
Total	**24**

Table 2: Format for the 24 bits of Level 1 data prepared by the HTR cards.

4.3 Level 2/DAQ Path

As mentioned in section 4.1, all data enters both the Level 1 and Level 2 /DAQ paths in parallel, and data consists of 16 bits HCAL energy **(or ET?)** and 2 bits for cap and frame errors. Figure 5 shows a schematic of the Level 2/DAQ path. Data is first put into RAM awaiting a Level 1 decision from the Level 1 framework. **(is it here that we would use the error bits to zero the energy before summing? if so, then do we need to continue to carry the extra 2 bits through to the derandomizing buffers? after summing? how does the level 1 decision get into the card? what kind of protocol? copper or fiber? and what is the nature of the l1 decoder?)** A decoder will determine from the level 1 answer, beam counter signal, and pipeline delay which data is associated with which level 1 accept, producing a address pointer to the RAM for the HCAL channels. An appropriate set of 10 data values will then be moved into a “derandomizing buffer” which serves as a vector buffer holding all 10 data

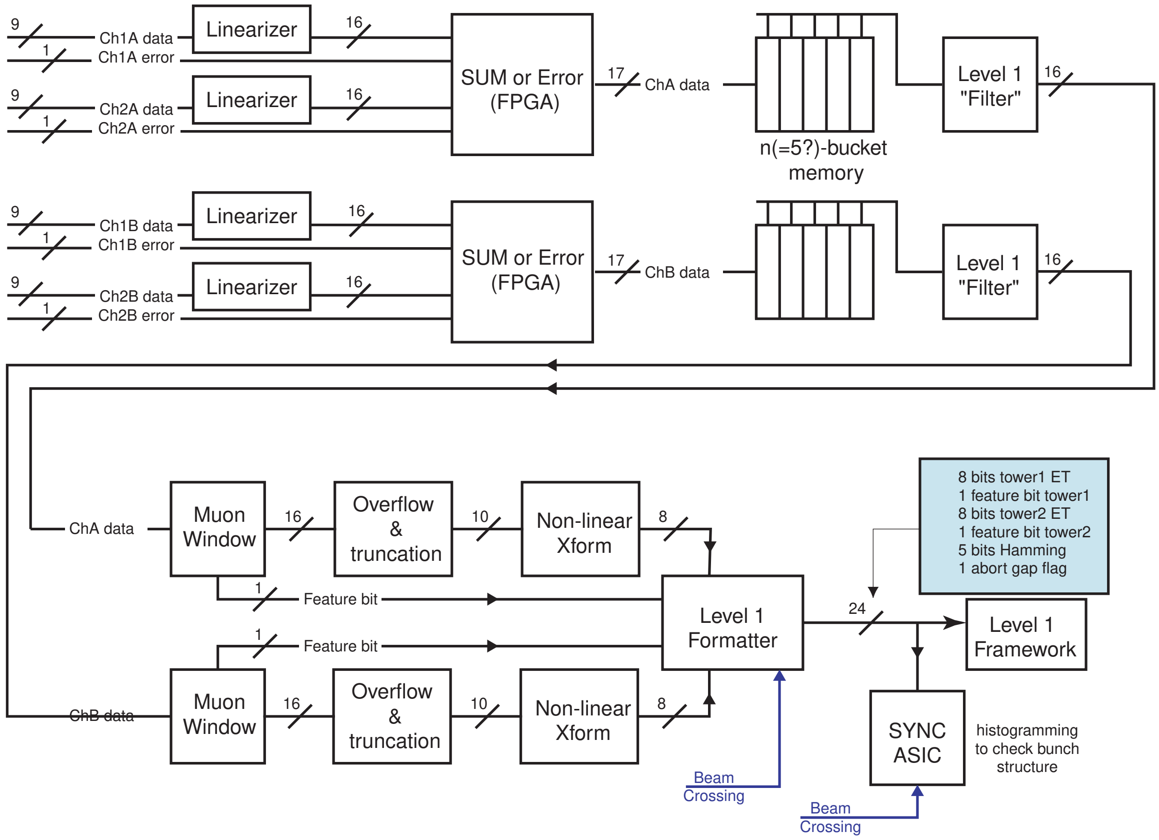

Figure 4: HTR Level 1 Path.

values and associating these values with a particular level 1 accept. This buffer will have to be able to hold 10 channels of 18 bits each and some number of level 1 accepts. The architecture of the HTR card will have all 32 channels' derandomizing buffers read out over a common internal data bus, and passed into a Level 2 filter which has the same function as that for Level 1, with more precision (hence the need for the additional 5 HCAL channels) Level 2 filter constructs the appropriate sum, the data is ready for formatting and sending to Level 2/DAQ. Each of these components are discussed below.

4.3.1 Derandomizing Buffer

4.3.2 Level 2 Filtering

As discussed above, the Level 2 filtering is expected to be more precise than that use for Level 1. The filter will use as its input the values of a single channel for some number of buckets, and combine them into an energy **(ET?)** and associate that energy with a particular beam crossing. The filter will have the form:

$$\text{Output} = \sum_{i=1}^{N} w_i D_i$$

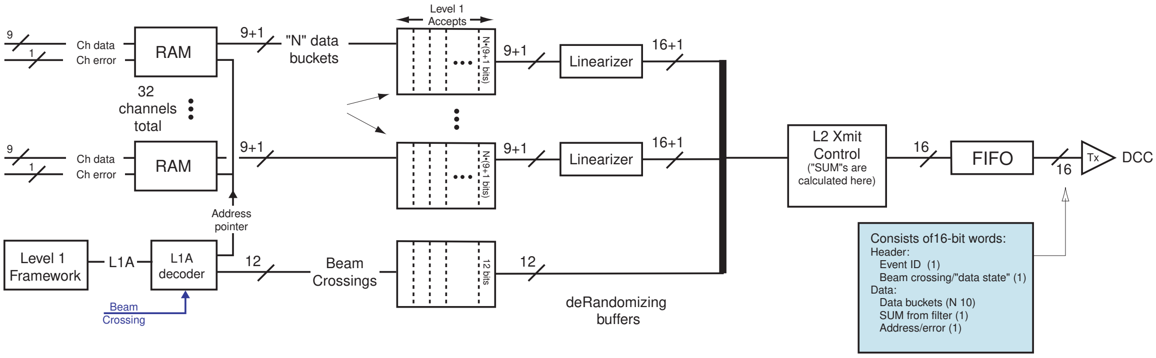

Figure 5: HTR Level 2/DAQ Path.

where N is the number of channels involved in the sum (*e.g.* 10), w_i corresponds to the weights and D_i corresponds to the 16 bit sum in channel i. For instance, for the Level 1 filter, $N = 5$, $w_1 = w_2 = w_3 = 1.0$ and $w_4 = w_5 = -1.5$. A Monte Carlo study will determine the optimum weights and number of channels. Note that we plan to implement this filter using the ECAL ASIC **(i need references for this!!!)**

4.3.3 Level 2/DAQ Control and Formatting

5 The HRC Card

6 The DCC Card

The Data Concentrator Card (DCC) receives data over 18 serial links from the HTR cards (one per HTR card) , performs error-checking and monitoring, and transmits the data to the CMS DAQ via the optical Front-End Link (FEL) in large blocks of roughly 1000 events. The DCC contains event-building logic, extensive error-checking and monitoring logic, and data buffering and formatting logic.

The DCC together with some logic on the HRC perform the functions known as FMU (Fast Monitoring Unit) and DDU (Detector-Dependent Unit) in CMS TriDAS jargon.

he DCC is constructed of a generic 9U VME motherboard, six 3-channel serial Link Receiver Boards (LRBs), a logic board, and a front-end link (FEL) transmitter on a PCI bus mezzanine card (PMC)[2] provided by the CMS TriDAS group. Clock and trigger synchronization signals (from the TTC) are received over a cable from the HRC card described in Section 5.

The event data is also available to be read by a processor card using VME for purposes of debugging and monitoring. This is done in a non-intrusive way, in order not to interfere with data taking. Events are copied into a dual-port memory, where they can be collected by a controller in the crate. In order to avoid adding dead time by the process of copying memory, this is done simultaneously with the data being transmitted to DAQ, using some predefined algorithm such as “copy a sequence of events”, or “randomly copy this event”.

6.1 Inputs and Outputs

The following inputs and outputs are foreseen in the DCC:

HTR Input Links are implemented using a standardized link receiver board (LRB). Each DCC may contain up to 18 link receivers on six 3-channel LRBs. The physical links are 28 bit LVDS serial links carried on a 10-conductor twisted pair cable.

Synchronization Signals are received on a four-pair cable from the HRC. This cable delivers the 40.08 MHz LHC bunch crossing clock plus the bunch counter reset, event counter reset and level 1 accept signals. The synchronization receiver may be mounted on the DCC logic board directly.

FEL Output Link to the CMS DAQ is a fiber optic link capable of roughly 400Mbytes/sec. The link transmitter itself will be a design supplied by the CMS TriDAS group. The interface is currently foreseen to be a PMC site provided on the DCC.

Trigger Data Link to the CMS trigger data concentrator is a point-to-point link to a crate which reads out the trigger system "as a detector." The nature of this link is *t.b.d.* The principle is that all data which is transmitted to the level 1 trigger system is sent (for triggered events only) via this link. In addition, *all* data may optionally be sent to this link (at a reduced data rate) for diagnostic purposes.

FMU Signals. A summary of errors and other monitoring information (buffer occupancies, *i.e.*) is gathered on the DCC and transmitted in "real time" to the HRC. The nature of this link is *t.b.d.*

Backplane Connectors A VME interface is provided for initialization, control and monitoring. It is anticipated that we will use VME64x[3] features and in addition some features of VME64xP (VIPA)[4]. The VME64x standard defines use of the J1 and J2 connectors for VME64 data transfers, plus additional ground and user-defined pins on J2. In addition, J0 (located between J1 and J2) will be used for additional 3.3V power and user-defined signals.

It is not currently foreseen to use the J3/J4/J5/J6 sites in the DCC.

JTAG Connector Although we still are not sure whether to do a complete implementation of JTAG in the DCC (i.e. whether to design the DCC so that it can be fully testable with JTAG), this bus still needs to be implemented as most FPGAs now can be programmed by JTAG on-board. Adding extra testability, although highly desirable, implies the development (or purchase) of testing software to go with it.

One possibility for implementation of this connector is to make it compliant with Altera's ByteBlaster connector, which also supports JTAG. It is very likely that this will be the main use of this protocol.

The JTAG bus may also be available from the backplane, through dedicated pins. This would allow an external controller to access the board for any tests that may need to be done.

6.2 DCC Architecture

A simplified diagram of the DCC is shown in Figure 6.

6.2.1 Link Receiver Boards

Data is received by six 3-channel LRBs implemented as PC-MIP[1] modules, each with a 32-bit, 33MHz PCI bus interface. Event data is received as a block from each HTR into a FIFO on the LRB, with one block being transmitted in response to each level-1 accept. Each group of three

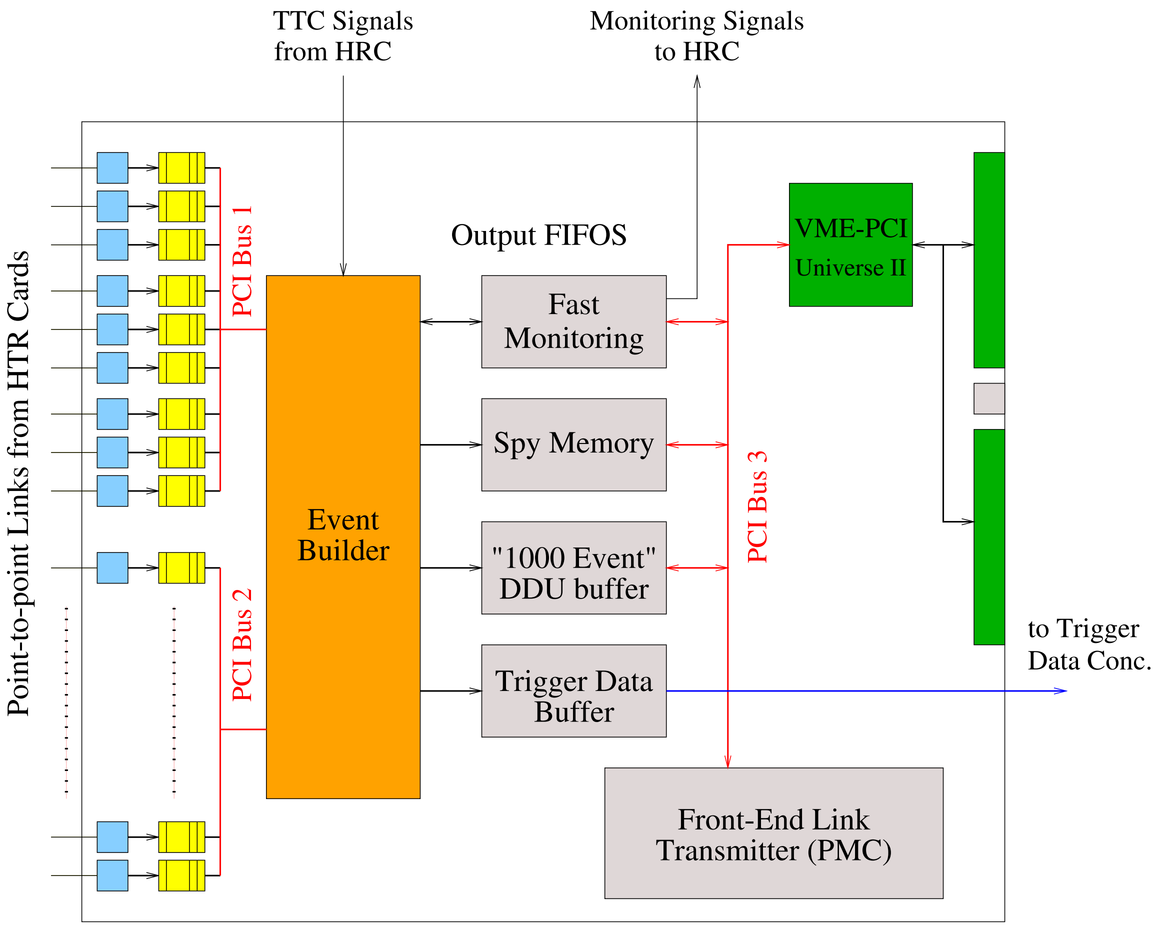

Figure 6: **DCC Block Diagram.**

LRBs (nine input links) is connected to the DCC logic board by a 32 bit PCI bus. Each event is read out from all LRBs on a PCI bus by a single PCI bus block read which deposits the data in an input buffer on the logic board.

The LRB provides the following processing and error-checking functions:

- Receive data blocks and check format (header, data, trailer) and size.
- Provide "ready" signal when all LRB buffers contain at least one complete block.
- Combine data from links across several LRBs into a single block in response to a PCI block read.
- Check event ID against an ID provided in the PCI address.
- If error occurs (data format error, ID mismatch, timeout, etc) flag the error in the block trailer.
- If impending buffer overflow, substitute error marks for data.

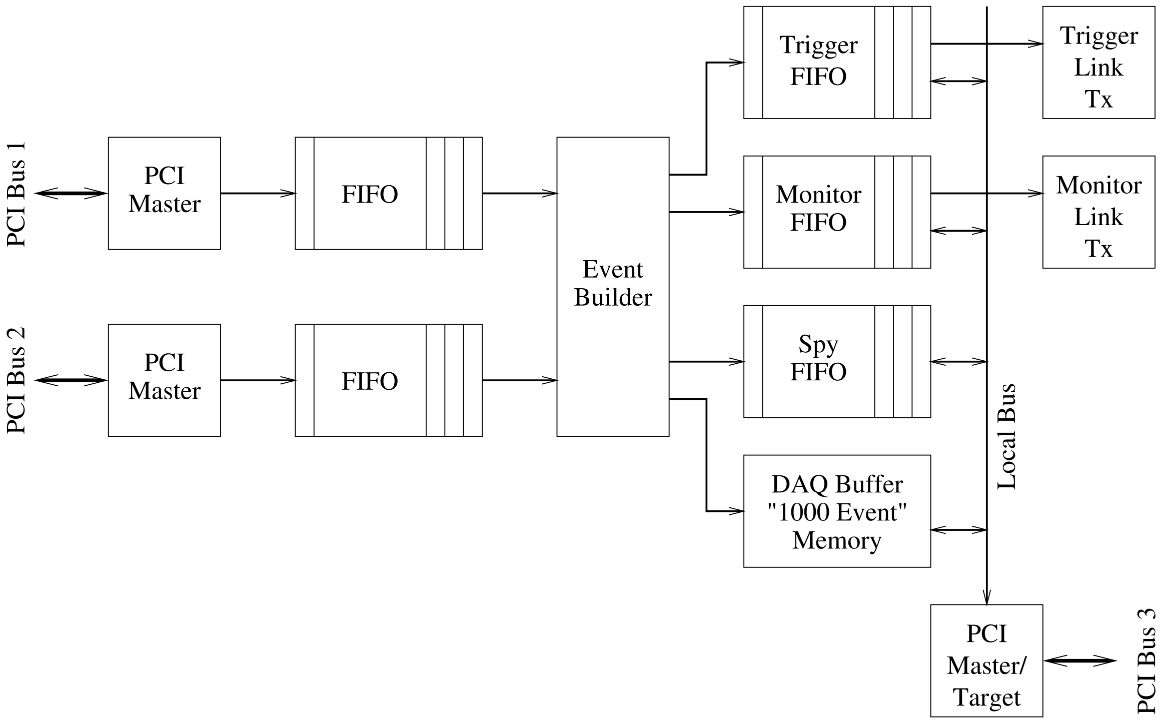

Figure 7: **DCC Logic Board Block Diagram**

6.2.2 DCC Logic Board

The core DCC functionality is implemented on a triple-size PMC type mezzanine card (see Figure 7). Three PCI bus masters provide the primary external interfaces, operating as described above. Data is read from busses 1 and 2 in parallel, then the two data streams are merged into single event blocks by an event builder. The data is further checked for errors and formatted into complete event blocks, which are written to 4 destinations simultaneously:

1. The "1000 event" output buffer memory, which is the primary path for DAQ data. This buffer is emptied via a large PCI block transfer to a memory on the FEL transmitter board. The details and protocol for this transfer are *t.b.d.*.

2. A Spy memory, which holds a sample of complete events for local readout over the VME bus. The logic board contains a small FIFO which is designed to hold a few events for transfer to a large memory on the VME motherboard. This path can be used for readout of all events using a local DAQ for diagnostic purposes.

3. The fast monitoring logic, which keeps real-time monitoring data such as histograms of event sizes, etc. This data is transmitted to the central fast monitoring unit on the HRC board by an as-yet undefined signal path.

4. The trigger data link. All data marked as level 1 primitives by are copied from the data stream and sent to this link transmitter.

All 4 of the above memories are accessible for read/write from PCI bus 3 for diagnostic purposes.

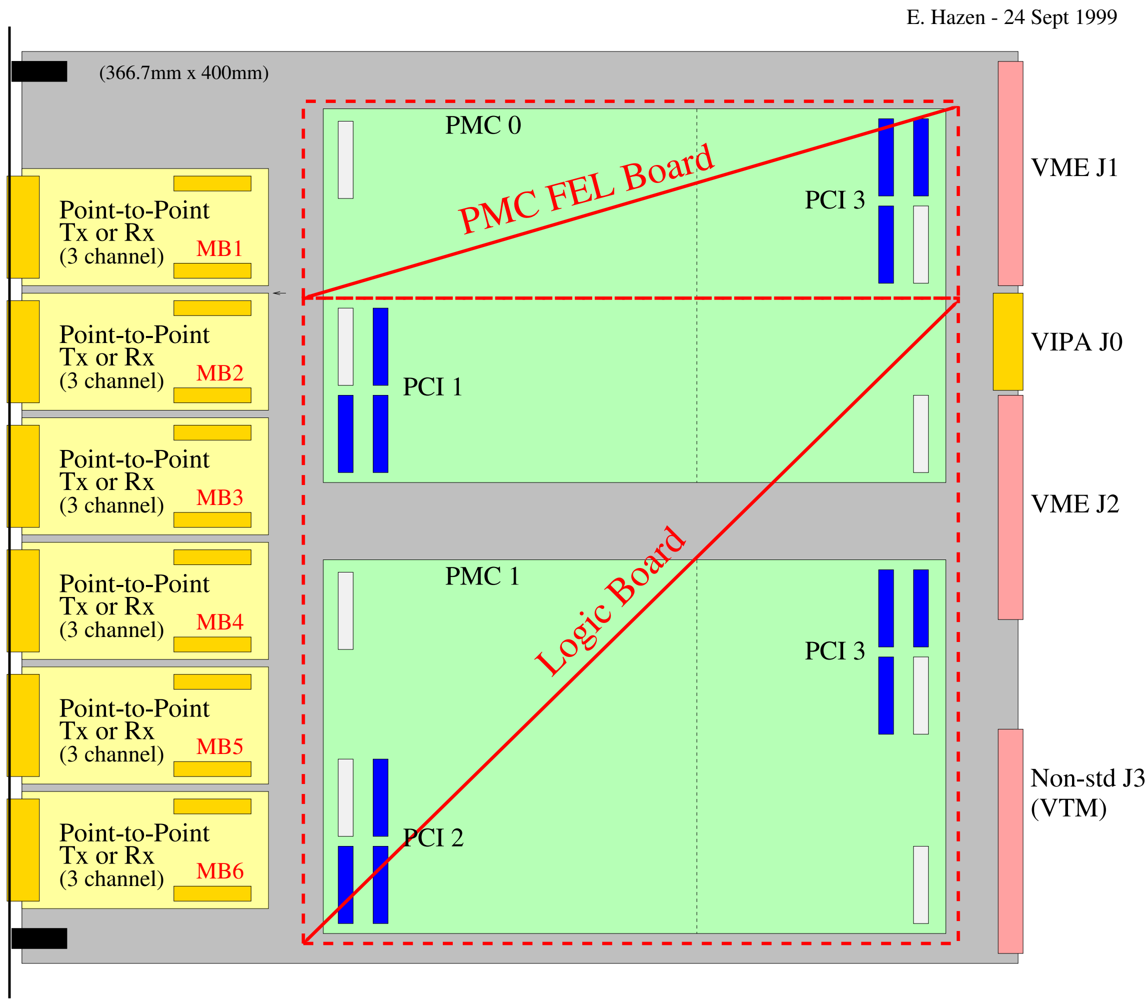

Figure 8: **VME Motherboard Layout**

6.2.3 Motherboard Implementation

The DCC is built on a "generic" 9Ux400mm[5] motherboard described in detail elsewhere[6]. The motherboard holds the link receiver PC-MIP and logic PMC mezzanine boards, VME-PCI and PCI-PCI bridge logic, dual-port and FPGAs. A mechanical sketch of the motherboard is shown in Figure 8, while a block diagram is shown in Figure 9

The motherboard can accommodate 4 PMC mezzanine boards or various combinations of over-sized boards which occupy more than one PMC site. For the DCC, we propose to use a triple-size board for the DCC logic, leaving a single, standard PMC site for the FEL transmitter (see Figure 8). All size PC-MIP sites will be occupied by LRBs to implement the 18 point-to-point link receivers.

The motherboard has 3 PCI busses which are bridged to each other and to the VME bus. During data-taking operations, all 3 PCI busses operate independently. Busses 1 and 2 are used to read events from the LRBs under control of two PCI master controllers on the logic board, while bus 3 is used to transfer data to the FEL transmitter. Total data rate is currently estimated to be 200Mbyte/s, which is comfortably less than the maximum of 260Mbyte/s bandwidth of

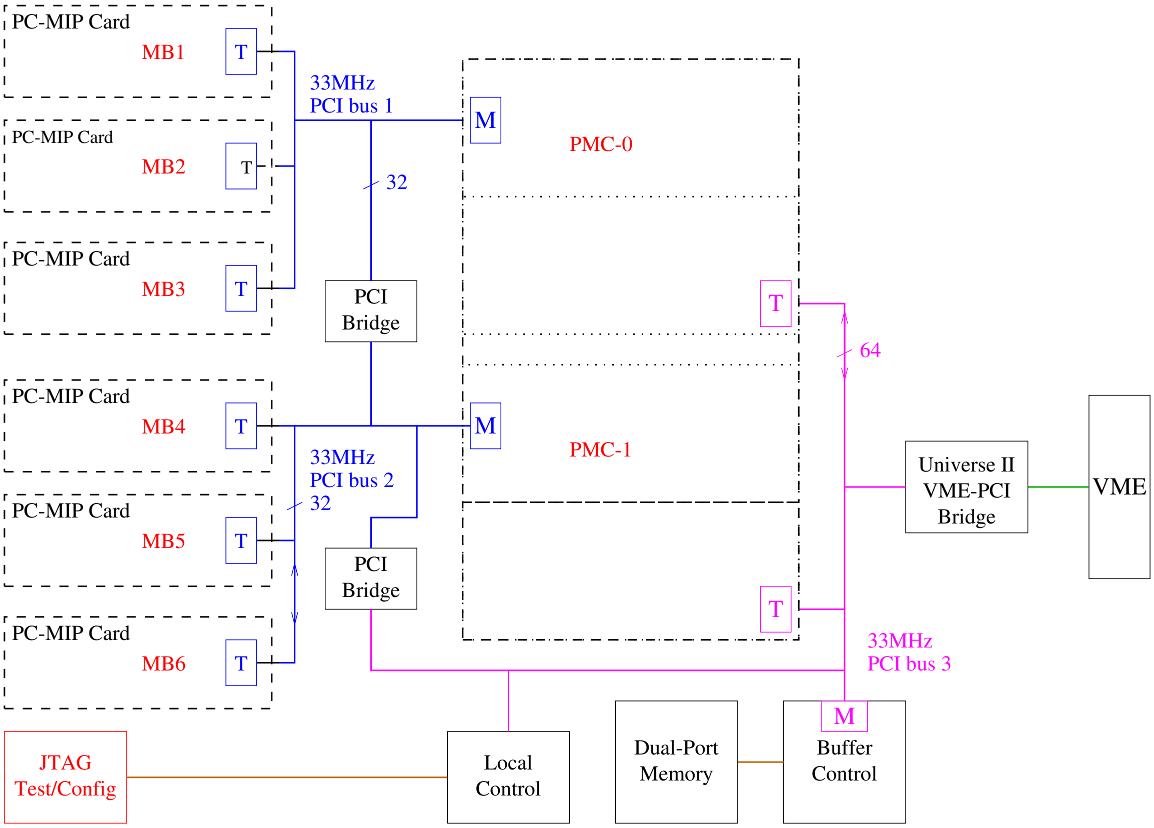

Figure 9: **VME Motherboard Block Diagram**

the 33MHz x 64 bit PCI bus 3.

The motherboard also contains a large dual-port memory accessible from PCI bus 3. This may be used for the Spy buffer and other slow monitoring data which is accessed from the VME bus.

Local control logic for JTAG access to motherboard components is provided via a local PCI target interface on PCI bus 3.

References

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[2] *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC.* IEEE P1386, 4/4/95 draft available at `http://ohm.bu.edu/~hazen/my_d0/std/pmc_draft.pdf`

[3] *American National Standard for VME64 Extensions.* ANSI/VITA 1.1-1997

[4] *VME64 Extensions for Physics and Other Applications* (VME64xP, *aka* VIPA). VITA 23-199x Draft of 2/1/99. Available at `http://ohm.bu.edu/~hazen/my_d0/std/VITA23-01FEB99.PDF`

[5] *American National Standard for VME64x 9U x 400 mm Format.* ANSI/VITA 1.3-1997

[6] *Waiting for a reference section from E. Hazen*

[7] *Waiting for the FNAL group's TDR on the QIE.*