HCAL TPG and Readout

CMS HCal meeting at Rochester Oct. 19-20 Oct 2001

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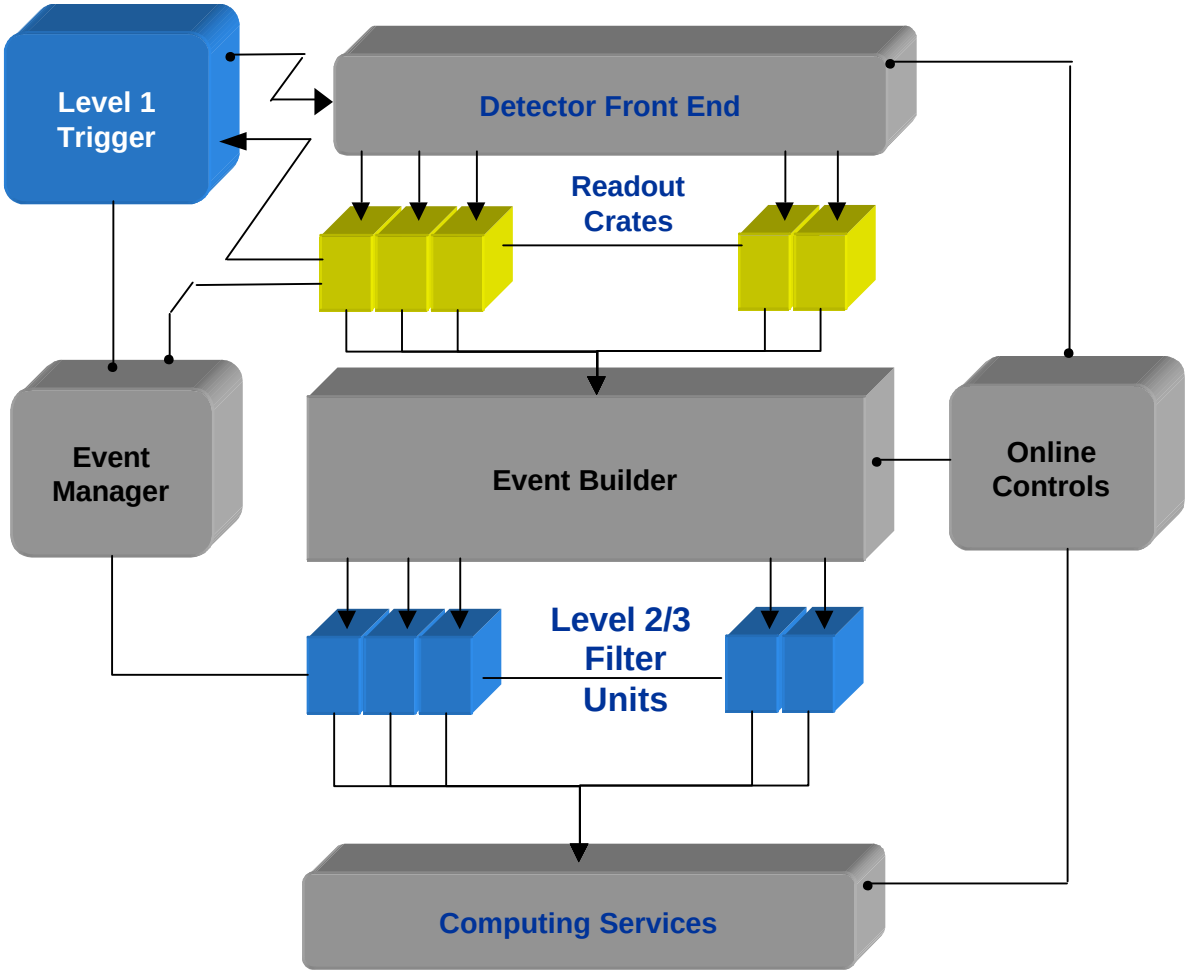
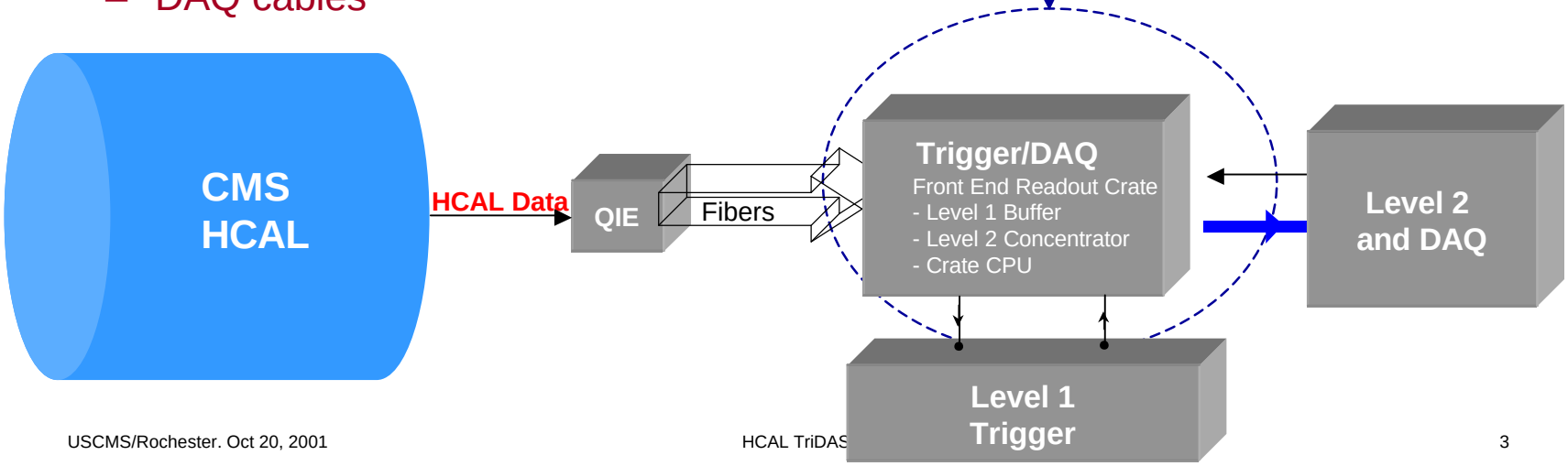
CMS TriDAS Architecture

- Data from CMS FE to T/DAQ Readout Crates
- Level 1 “primitives”
  - Crossing determined
  - Summing
  - Tx to Level 1 Trigger
  - Data is pipelined waiting decision
- Level 1 accepts cause
  - Tx raw data to concentrators
  - Buffered and wait for DAQ readout
- System communication via separate path (TTC)
  - Clock, resets, errors, L1 accepts…

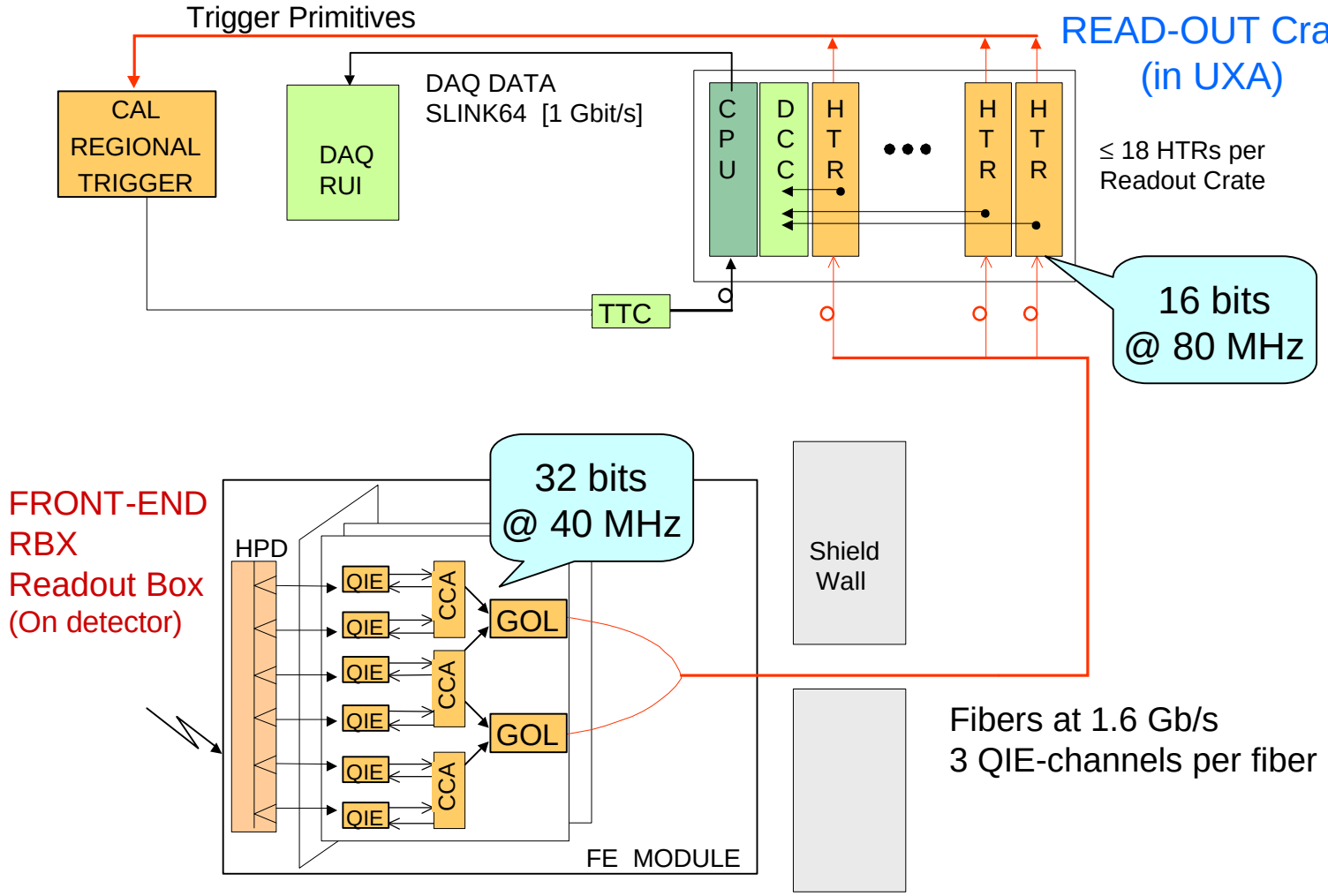


HCAL Contribution to T/DAQ

- Includes:
  - Receiver cards (including fiber input receivers and deserializers)
  - Cables to Level 1 Trigger system
  - Concentrators
  - VME crate CPU module
  - VME crates and racks
- Everything between but not including:
  - Fibers from QIE FEs
  - DAQ cables

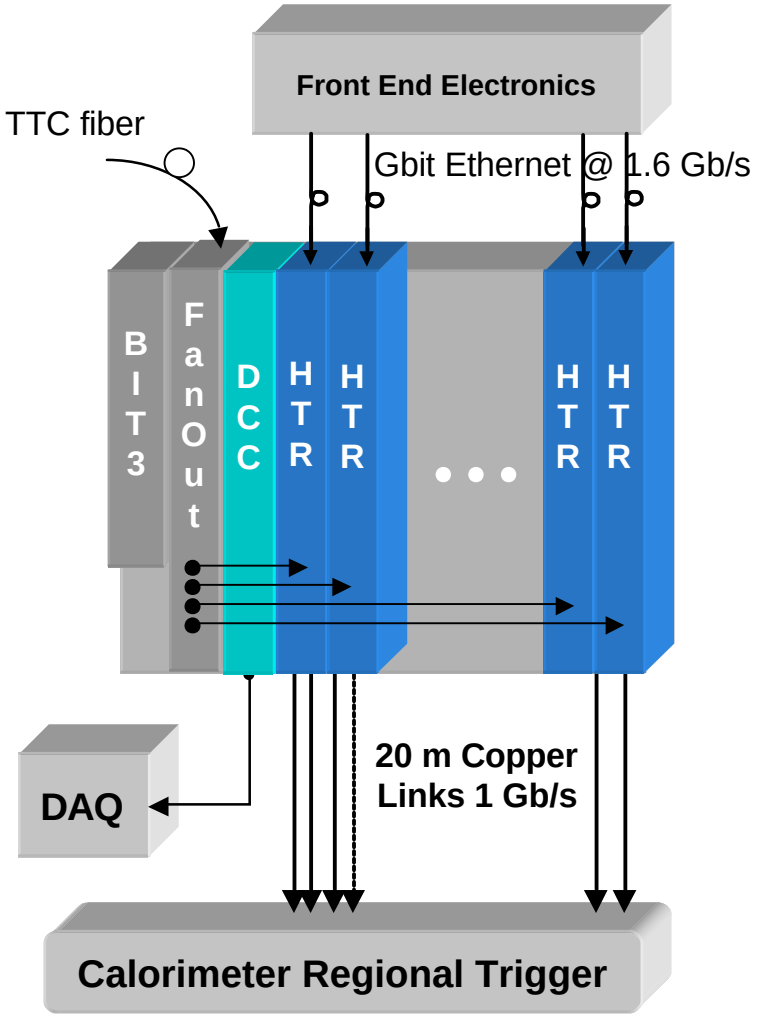


HCAL FE/DAQ Overview



Readout Crate Components

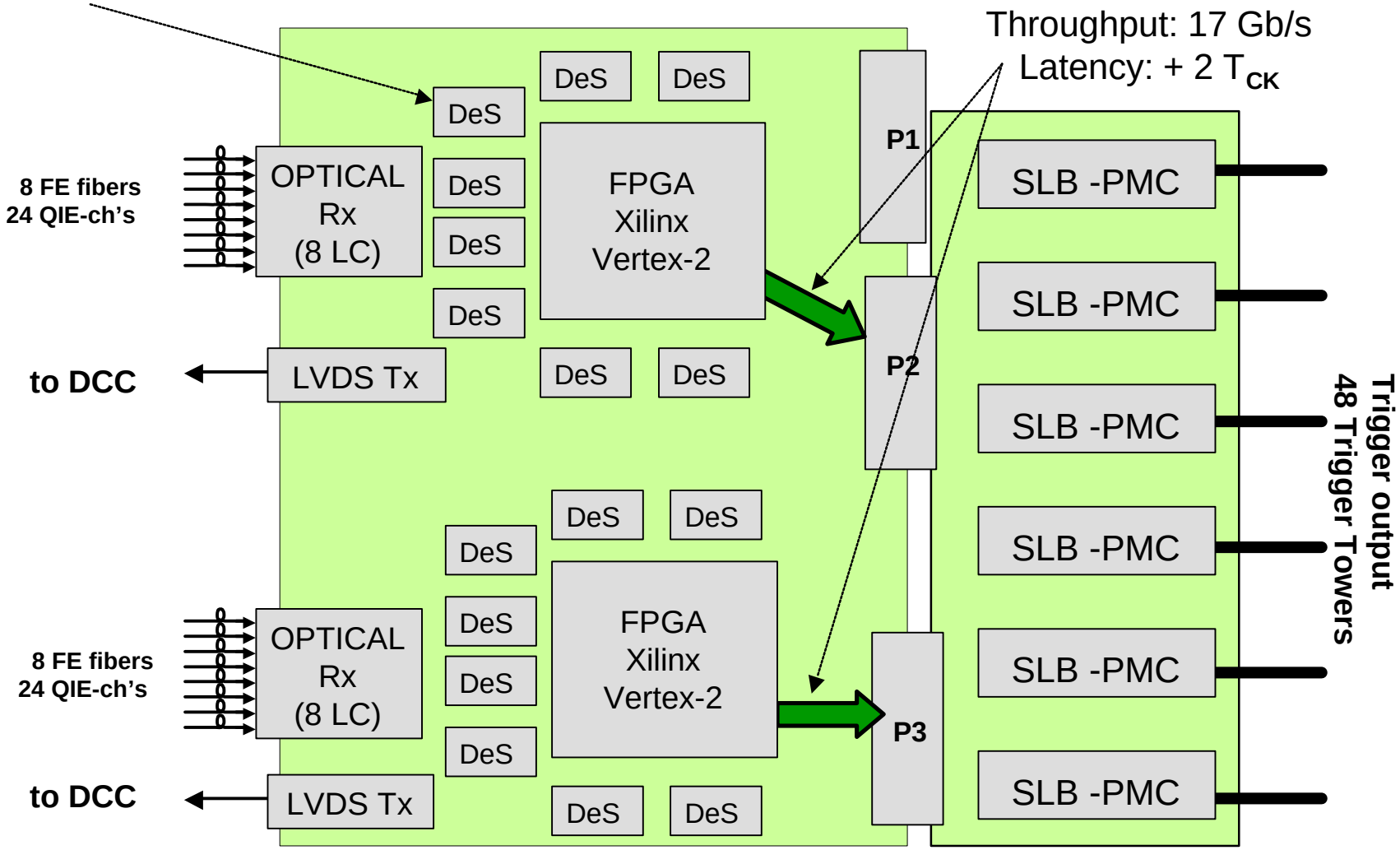
- **"BIT3"** board
  - Commercial VME/PCI Interface to CPU
  - Slow monitoring
- **FanOut** board
  - FanOut of TTC stream
  - FanOut of RX_CK & RX_BC0
- **HTR** (**H**CAL **T**rigger and **R**eadout) board
  - FE-Fiber input
  - TPs output (SLBs) to CRT
  - DAQ/TP Data output to DCC
  - Spy output
- **DCC** (**D**ata **C**oncentrator **C**ard) board
  - Input from HTRs
  - Output to DAQ
  - Spy output



HCAL TRIGGER and READOUT Card

- I/O on front panel:
  - Inputs: Raw data:
    - 16 digital serial fibers from QIE, 3 HCAL channels per fiber = 48 HCAL channels
  - Inputs: Timing (clock, orbit marker, etc.)
    - LVDS
  - Outputs: DAQ data output to DCC
    - Two connector running LVDS
- TPG (Trigger Primitive Generator, HCAL Tower info to L1) via P2/P3
  - Via shielded twisted pair/Vitesse
  - Use aux card to hold Tx daughterboards
- FPGA logic implements:
  - Level 1 Path:
    - Trigger primitive preparation
    - Transmission to Level 1
  - Level 2/DAQ Path:
    - Buffering for Level 1 Decision
    - No filtering or crossing determination necessary
    - Transmission to DCC for Level 2/DAQ readout

HTR – "Dense" scheme



“Dense” HTR

- Strong reasons to push to dense scheme
  - Money
    - Fewer boards!
  - Programmable logic vs. hardware
    - Avoid hardware MUXs
    - Maintain synchronicity
  - Single FPGA per 8 channels
    - Both L1/TPG and L1A/DCC processing
    - Xilinx Vertex-2 PRO will have deserializer chips built in!
      - Saves $500/board
      - Many fewer connections
      - ~20 DeS->FPGA connections replaced by 1 1.6 GHz line
      - Challenges:
        - » Layout of 1.6 GHz signals
        - » Schedule implications for final production may have to slip ~6 months to wait for Vertex-2 PRO
- What do we give up?
  - Each board much more epensive
  - More difficult layout
  - Need transition board to handle TPG output
    - So does ECAL – common solution will be used
  - Need 2 DCC/crate (but half the number of crates!)

Changes from HTR Demo to Final

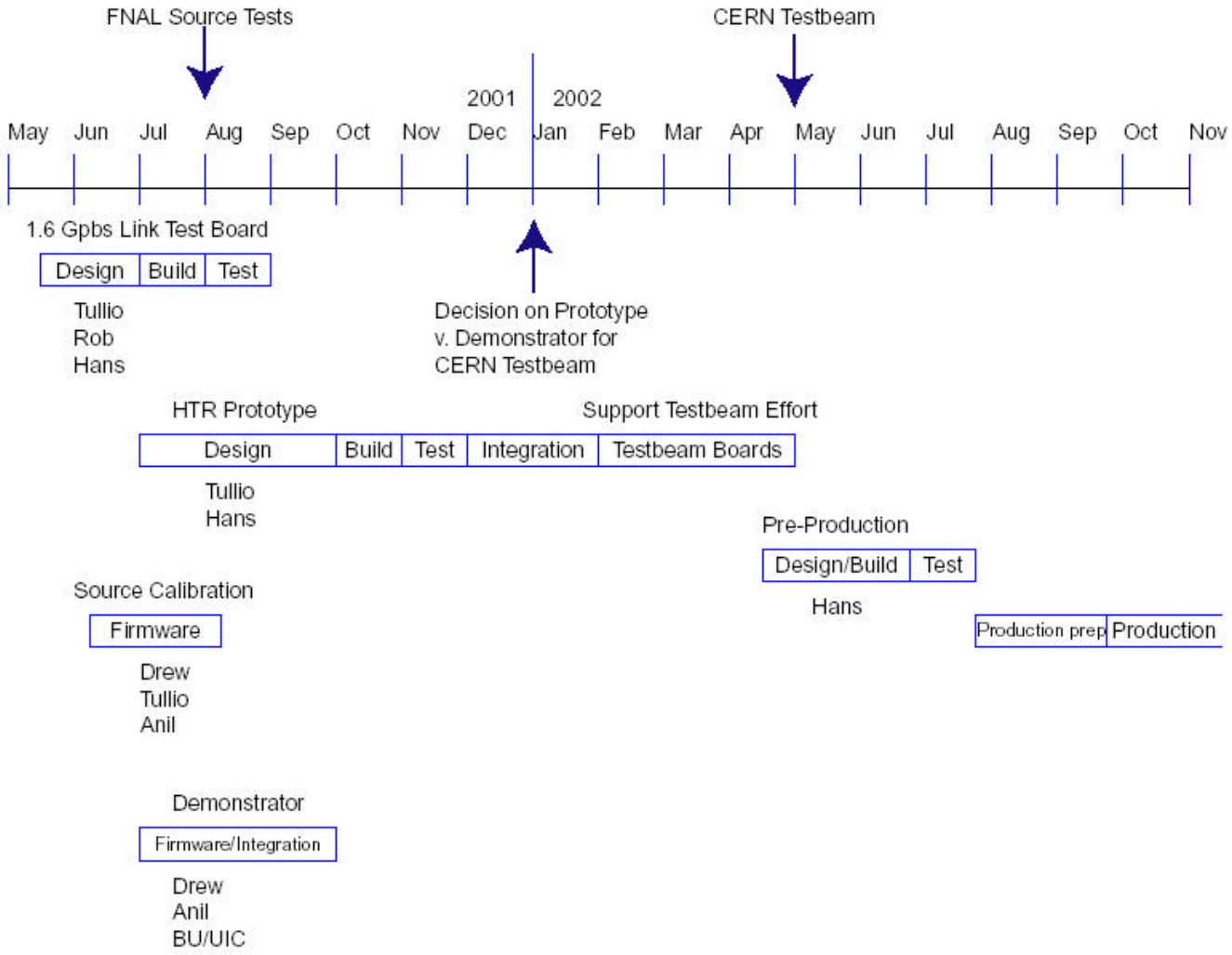
- Front-end input
  - From 800MHz HP G-Links to 1600MHz TI Gigabit ethernet
- Timing
  - TTC daughterboard to TTC ASIC
- Core logic
  - Altera to Xilinx
- Trigger output
  - Moved to transition board
- Form factor
  - 6U to 9U

Output to DCC? Unchanged!!!

Status

- Front-end emulator ⇒HTR demonstrator ⇒ DCC ⇒ S-Link ⇒ CPU
  - Successful operation of each individual link
    - Integration underway - Tullio goes to Boston next week
- Pre-prototype board layout
  - Complete, board is now being stuffed
  - Will have only 1 FPGA with full complement of associated parts
    - Will use the TI Deserializers – not the Vertex 2 PRO
  - Internal use only
- Prototype layout
  - Should be complete in November
    - Some changes from pre-prototype, but minor
- Maryland activity is in prep for source tests and 9U board design
  - Preparation for testbeam summer 02 not yet started
  - Trying hard to meet March 02 deadline for decision on which HTR to use for testbeam
- Energy filters still undefined

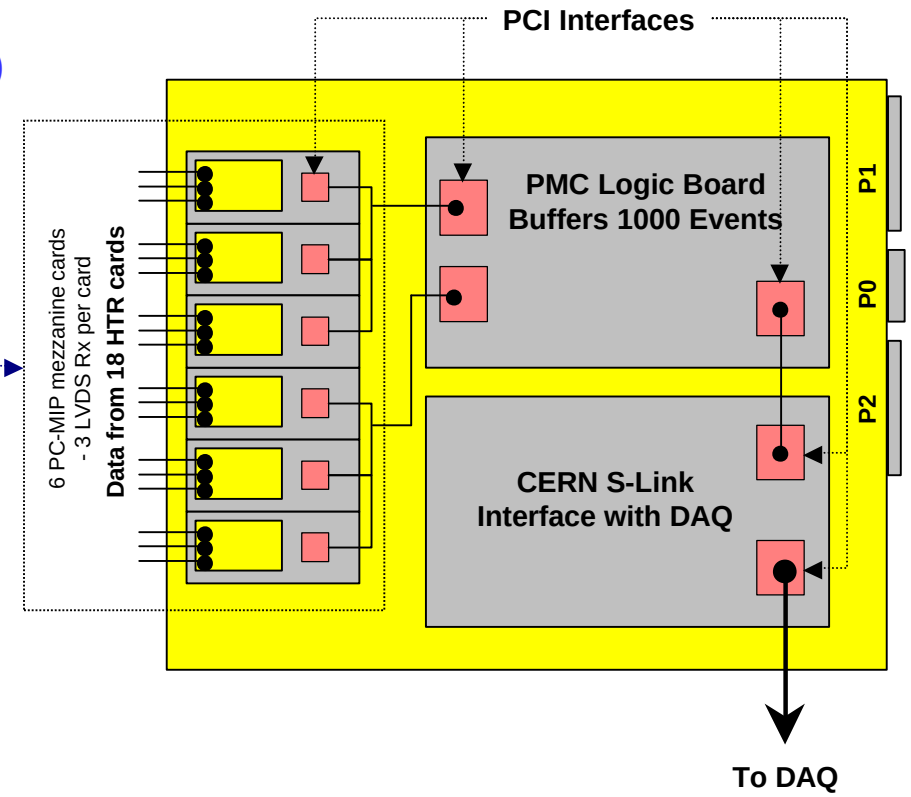
Current HTR Timeline



DATA CONCENTRATOR CARD

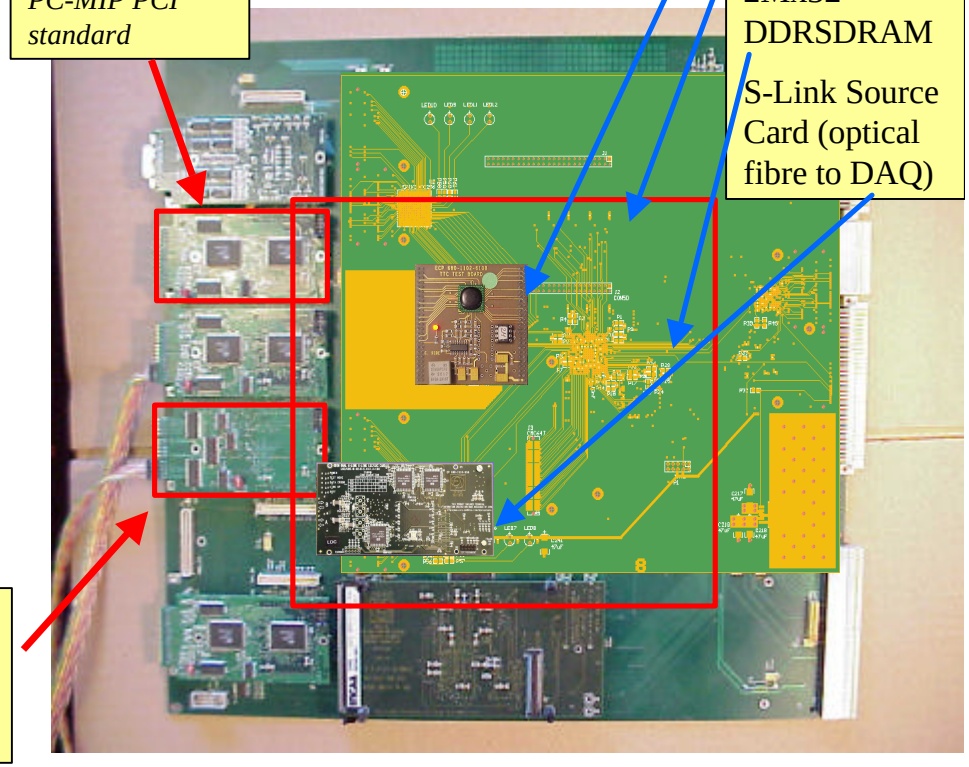
Motherboard/daughterboard design:

- Build motherboard to accommodate
  - PCI interfaces (to PMC and PC-MIP)
  - VME interface
- PC-MIP cards for data input
  - 3 LVDS inputs per card
  - 6 cards per DCC (= 18 inputs)
  - Engineering R&D courtesy of DÆ
- 1 PMC cards for
  - Buffering:
- Transmission to L2/DAQ via CERN S-Link Tx
  - http://hsi.web.cern.ch/HSI/s-link/



Project Status Details DCC@BU

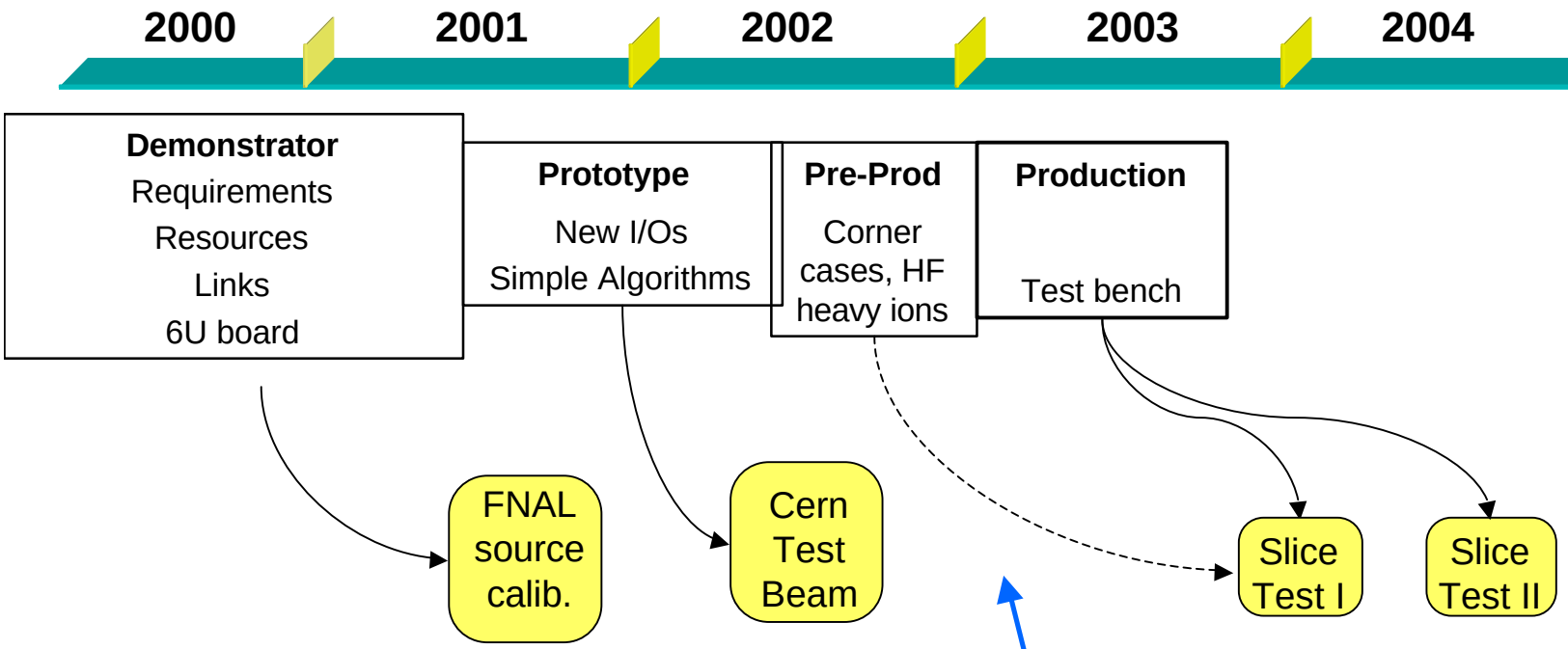
- VME Motherboard
  - Two prototypes working; 5 more boards being built
- Link Receiver Board (LRB)
  - 10 second-generation boards working
- DCC Logic Board
  - PCB Design complete; being fabricated
  - FPGA coding underway
- Test Stand Hardware Complete
  - Pentium/Linux computer, TTC System Working
  - Link Transmitters to simulate HRC working
  - S-Link cards available



HCAL TIMING FANOUT Module

- Fanout of TTC info:
  - Both TTC channels fanout to each HTR and DCC
  - Separate fanout of clock/BC0 for TPG synchronization
    - “daSilva” scheme
- Single width VME module

Current Project Timeline



Pre-prod too short: not useful

Test bench before production ?

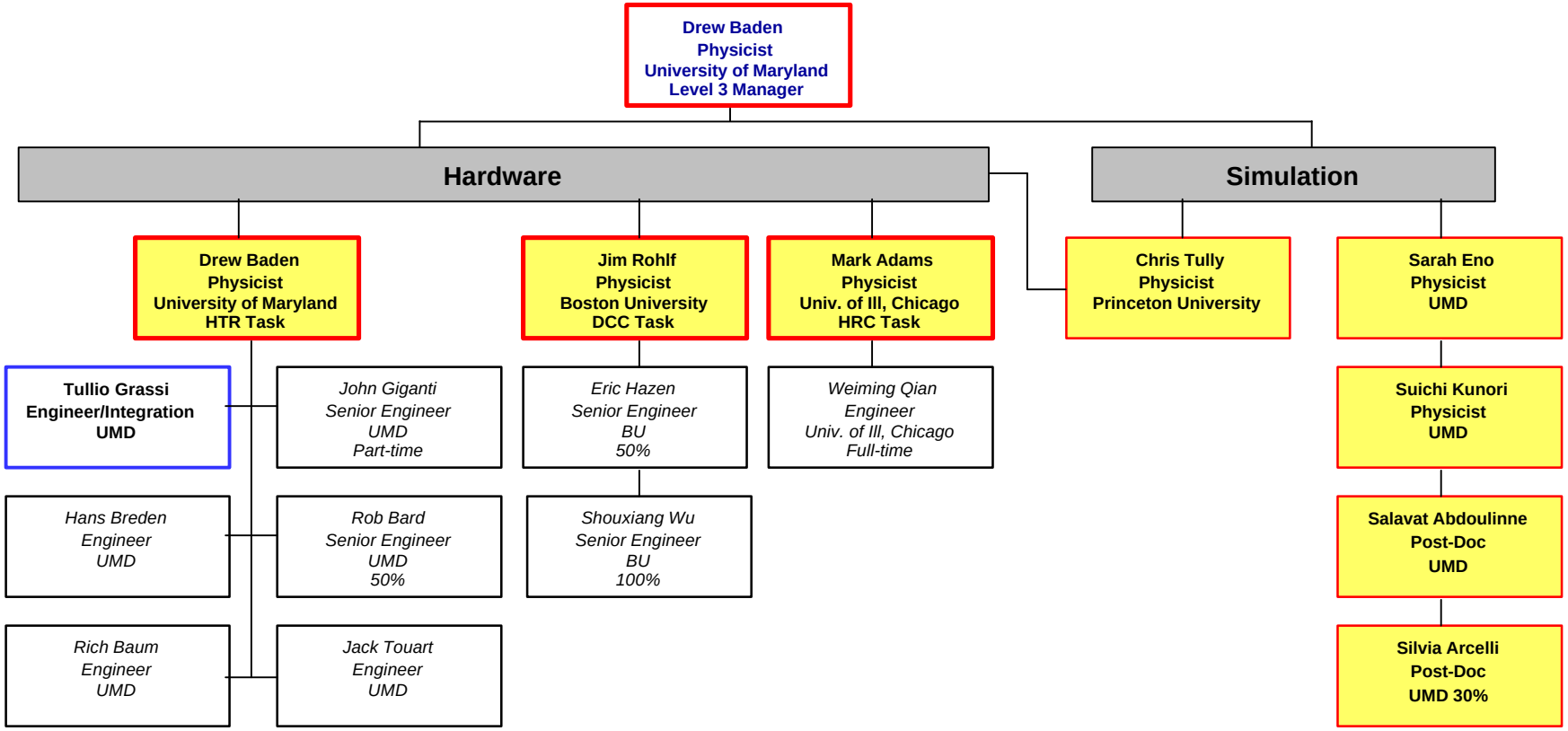
Slice Test I with pre-production ?

Vertex-2 PRO?

STILL SOME UNCERTAINTIES…

Manpower

- All Engineering/technical identified and on board.



Project Status Summary

- HTR (Maryland):
  - 6U Demonstrator built and under test
    - 800 Mbps G-Links works fine
    - Integration with FEE and DCC underway
  - 9U pre-Prototype layout done
  - 9U Prototype layout underway
    - Still a few issues to decide
      - 1.6 Mbps link
      - FPGA choice (Vertex-2 vs Vertex-2 PRO)
      - Link to Level 1 trigger
    - Plan to have this board on the test bench by Dec '01
- "HRC"
  - UIC engineer onboard April '01
  - Requirements have decreased, card will be easy to complete
- DCC (BU)
  - DCC 9U motherboard built and tested ≡ finished
    - PCI meets 33MHz spec
    - Card is done!
  - Link Receiver Cards built and tested
    - Done
  - PMC logic board
    - First version complete
    - FPGA and etc. underway