VME FPGA
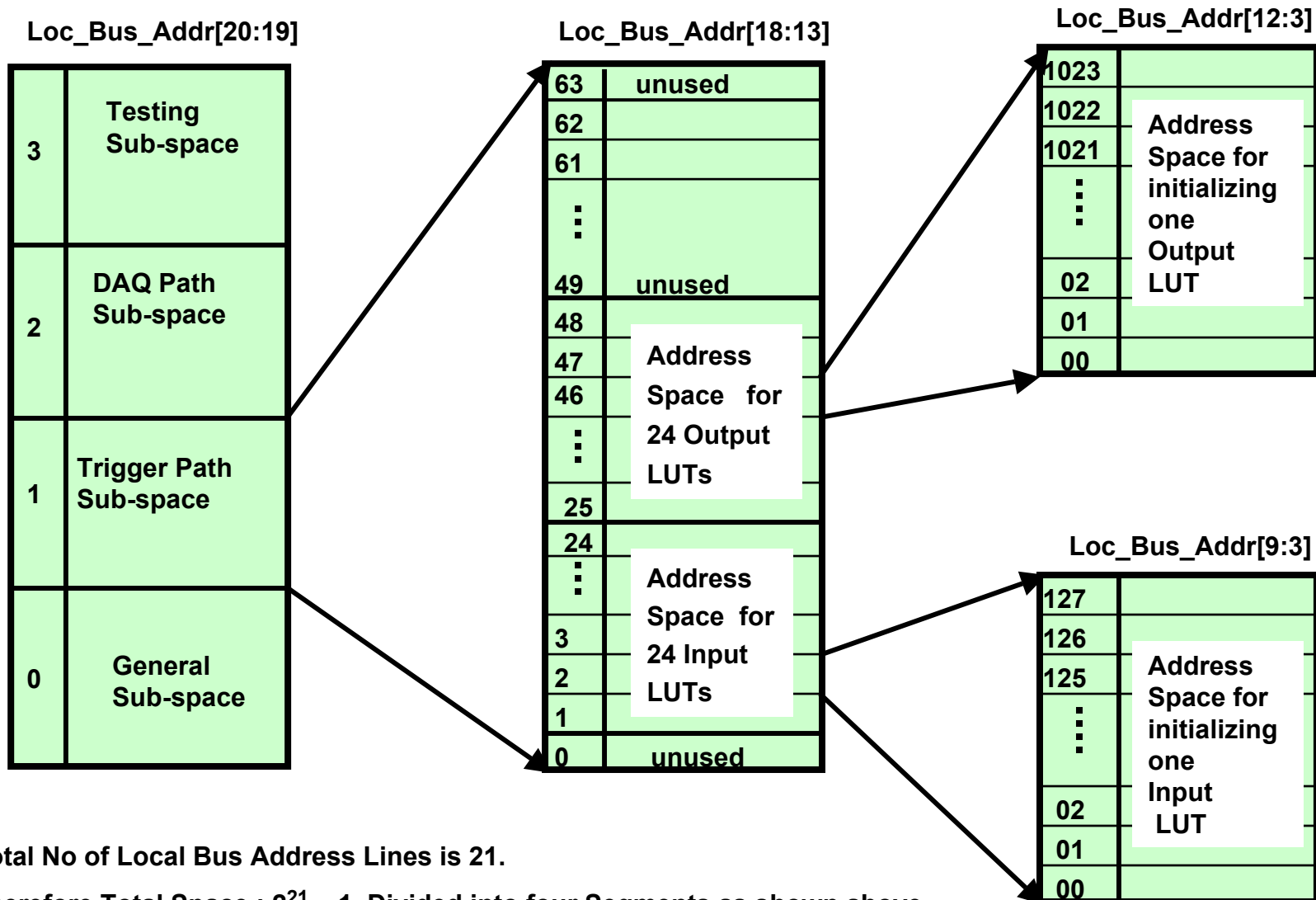
List of changes from the VME FPGA in the HTR prototype, see document and code available from the HTR proto web page.

1) comply to CMS rules

2) The FPGA chip is now an Altera Acex EP1K50QC208-3 208-Pin PQFP

3) The flash memory device is now Am29LV116D from AMD; it has one more address line (and twice the memory)

4) Loading of LUTs for trigger-path: each LUT is seen as a single address by the CPU (in order to reduce the CPU memory space); but the Main FPGA (Xilinx) assigns one address per each location.
The VME FPGA (Altera Acex) has the task to generate the correct sequence of LocalBus addresses when the VME issue the address of an LUT. The process imply that the CPU generates a number of consequtive accesses (equal to the LUT size, that is 128 for the Input_LUT and 1024 for the Output_LUT) at the same address, but with different data (the data sequence to be loaded in the given LUT). The Main FPGA address map is shown on the next page.

5) Some individual registers will be added or updated (Input_Delay, etc).

6) The SLBs are six new LocalBus slaves. Details are on paragraph 4 of "Specifications of the Synchronization and Link Board PMC Version (SLB-PMC)" , available at: http://tgrassi.home.cern.ch/tgrassi/hcal/SLB_PMC_spec.pdf

Address Section in Xilinx Main FPGA

Loc_Bus_Addr[20:19]

3	Testing Sub-space
2	DAQ Path Sub-space
1	Trigger Path Sub-space
0	General Sub-space

Loc_Bus_Addr[18:13]

63	unused
62	
61	
⋮	
49	unused
48	
47	Address Space for 24 Output LUTs
46	
⋮	
25	
24	
⋮	Address Space for 24 Input LUTs
3	
2	
1	
0	unused

Loc_Bus_Addr[12:3]

1023	
1022	Address Space for initializing one Output LUT
1021	
⋮	
02	
01	
00	

Loc_Bus_Addr[9:3]

127	
126	
125	Address Space for initializing one Input LUT
⋮	
02	
01	
00	

Total No of Local Bus Address Lines is 21.

Therefore Total Space : $2^{21} - 1$. Divided into four Segments as shown above

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