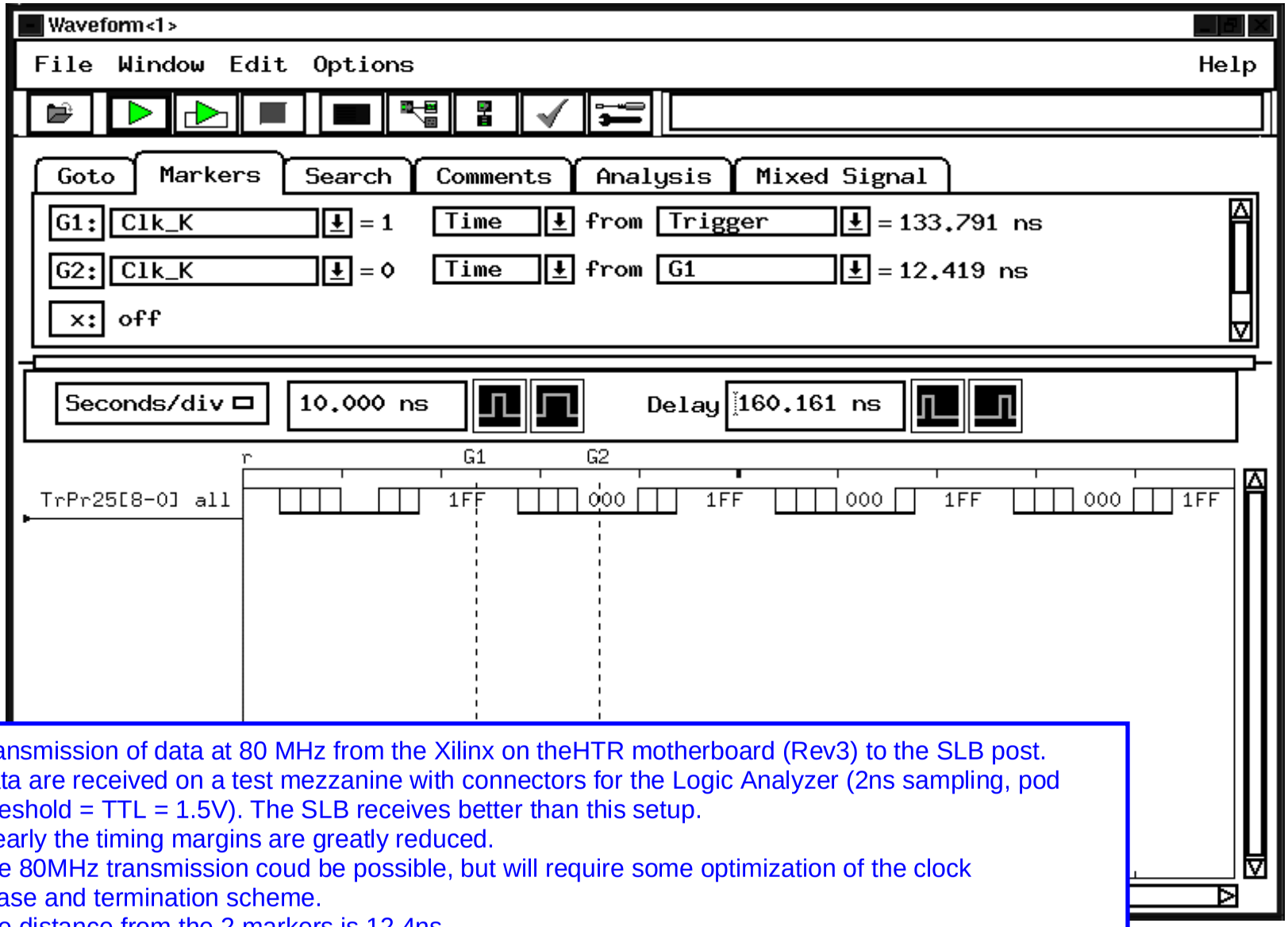

Transmission of data at 80 MHz from the Xilinx on theHTR motherboard (Rev3) to the SLB post. Data are received on a test mezzanine with connectors for the Logic Analyzer (2ns sampling, pod threshold = TTL = 1.5V). The SLB receives better than this setup.
Clearly the timing margins are greatly reduced.
The 80MHz transmission coud be possible, but will require some optimization of the clock phase and termination scheme.
The distance from the 2 markers is 12.4ns