

Waveform<1>

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G1: Clk_K ↓ = 1 Time ↓ from Trigger ↓ = 133.791 ns
 G2: Clk_K ↓ = 0 Time ↓ from G1 ↓ = 12.419 ns
 X: off

Seconds/div □ 10.000 ns Delay 160.161 ns

T-P+2518-01 all

Transmission of data at 80 MHz from the Xilinx on theHTR motherboard (Rev3) to the SLB post. Data are received on a test mezzanine with connectors for the Logic Analyzer (2ns sampling, pod threshold = TTL = 1.5V). The SLB receives better than this setup. Clearly the timing margins are greatly reduced. The 80MHz transmission could be possible, but will require some optimization of the clock phase and termination scheme. The distance from the 2 markers is 12.4ns