HCAL HTR Pre-Production board specifications

Last update: Jan 30, 2002 – Last Changes are in blue

The main use of this board is from May 2003 in Cern for Test beam and Slice tests.

In Cern are needed 11 boards + spares. In USA (UMD, BU, FNAL, Princeton) we need more boards to keep development. Thus we should produce about 25 boards.

1. Changes from prototype board

[compare with HCAL HTR Prototype board specifications and design guidelines available on:
http://www.physics.umd.edu/hep/tullio/proto/HTRproto_board_specs.pdf]

- add a TTC daughter card.
- add 6 SLBs on front-panel.
- The Front-Panel switches will be moved back and routed to the xilinx. The same for the sel line of the clock mux (Xtal or Clean_clk).
- JTAG an all devices that support it, possibly also for the programming of the gate arrays with the cable would be better with JTAG. Put jumper scheme to by-pass any device in the chain.
- on the VME FPGA there is an input clock from the VME back-plane. Replace it with a crystal oscillator. The reason is that this chip does not need synchronization with the rest of the board.
- Fiber input using the 8-channel passive Molex MTP Adapter on the front-panel and Stratos dual LC on board
- add stiffeners and possibly metal edges of the board.
- Connectors for Logic Analyzer in Local_Data, Local_Address, Local_other
- Every data connector of the SLB has half of its inputs from each of the 2 xilinx FPGAs.
- put ground "island" under all high-speed devices and clock drivers.
- The HTR prototype hangs up the bus when altera is not configured, find out why.
- In the unused portion of the board , put plenty of VCC and GND pads for reworking.

2. Board Input/Output

FE-Data Input

This data come on eight 100-meter optical fibers, 850nm, multimode 62.5/125 from the Cern GOL serializer to the MTP adapters. From there, there is an 8-way MTP-to-LC fanout going to the SFF dual LC receivers PN M2R-25-9-TL from StratosLightWave. The data-stream is on 1.6 Gb/s differential lines (DINRXP-DINRXN). Data are deserialized and 8B/10B decoded by eight TLK2501 parts (2.5V parts).

Timing Inputs

Timing signal are received via one RJ45 on a Cat 6E (or Cat7) cable. The TTC stream is a 160 MHz signal, RX_BC0 is a 40 MHz signal, RX_CLK is 40 MHz (jitter ~ 80ps pk-pk) and Clean_CLK is 80 MHz (jitter ~ 50ps pk-pk) . On clock signals the jitter should be minimized. The input connector is AMP 558342-1.

Pin	Signal		Pin	Signal
1	TTC-serial_P		2	TTC-serial_N
3	Rx_CLK_P (40 MHz)		4	Rx_BC0_P
5	Rx_BC0_N		6	Rx_CLK_N
7	CleanCLK_P (80 MHz)		8	CleanCLK_N

Table 1: Pin-out definitions on the RJ45 connector (pinning standard RG568B). All signals are 3.3V differential PECL.

The timing scheme is on a separate pdf document. Add buffers and terminations as needed.
RX_CLK and RX_BC0 have same length path to all SLBs (± 1 inch = 100 ps skew); the RX_BC0 pair go to the Xilinx chips to two adjacent pads: IO_LXX**P**_# and IO_LXX**N**_#, with XX a unique pair in the bank and # indicates the bank number (0 through 7).
The signals Brodcst[7:2], BrdcstStr, BcntRes, EvCntRes, L1A and Clk40Des1 come from the TTC mezzanine and go to the 2 xilinx chips and to the 6 SLBs. TTC_Reset_b and TTCready are routed to one xilinx chip only.
Add a pair Test_CLK+/- from two test points to two diff. GCLK input of each xilinx.

Connect TTCready and TTCreset_b to a xilinx.

L1-Trigger outputs

Those are 24 x 9 lines from each Xilinx FPGA. They will be source terminated inside the FPGA. This requires that the xilinx N reference pin (VRN) be pulled up to VCCO by a 50 Ohm reference resistor, and the P reference pin (VRP) must be pulled down to ground by another 50 Ohm reference resistor (1/10 watt or more).
The top xilinx send the following outputs:

TP1[8:0], TP2[8:0], …,TP24[8:0]

To these inputs of each SLB: Sync1_[8:0], Sync2_[8:0], Sync5_[8:0] and Sync6_[8:0]

The bottom xilinx to the connector 2 send the following outputs:

TP25[8:0], TP26[8:0], …, TP48[8:0]

To these inputs of each SLB: Sync3_[8:0], Sync4_[8:0], Sync7_[8:0] and Sync8_[8:0]

L2-DAQ-Data Output

The only change from the HTR prototype is that the output connector is RJ-45, 5 pairs.
The connector is made by Stewart, P/N SS-701010-NF, available from Arrow.
Driver-to-connector assignment is as on the top-right side of:
http://ohm.bu.edu/~hazen/my_d0/TxRx/ltb_2_5/LTB_sch.pdf

3. Main HTR FPGA

Candidates	*BRAM*	*I/O pins*	*Bitstream Length*	*$ (Avnet, >25pcs, Sep 02)*	*$ (Insight, ~100pcs Oct 02)*
XC2V2000-4BF957C	56	624	7,492,000 bits	590	472
XC2V3000-4BF957C	96	720	10,494,368 bits	930	743
XC2V4000-4BF957C	120	912	15,659,936 bits	1552	
XC2V2000-4FF896C	56	624	7,492,000 bits	590	
XC2V3000-4FF1152C	96	720	10,494,368 bits	930	
XC2V3000-4BG728C	96	516	10,494,368 bits	852	

Option 1) is our baseline. In case we need more resources options 1) and 2) are pin-out (footprint) compatible [Virtex-II handbook, page 42, Oct 2001].
Connect possibly ~4-wire switch, ~10 test points, ~2 LEDs to some unused pins.
Power connections: V_{CCO} = 2.5V; V_{CCAUX} = 3.3V.
Pin VRN must be pulled up to VCCO=2.5V by its 60 Ohm reference resistor. Pin VRP must be pulled down to ground by its 60 Ohm reference resistor.

4. VME FPGA: requirements and candidates

This FPGA will implement:
- The interface to the VME bus
- The configuration of the Main FPGAs and of the FLASH devices
- The master of the *Local Bus*

Requirement:
- 5V-tolerant
- System-gates: > 1000 Altera LCs
- No BGA
- No old parts

VME FPGA candidate devices:

Altera	Acex	EP1K30QC208-3	208-Pin PQFP	$17	
Altera	Acex	EP1K50QC208-3	208-Pin PQFP	$22	SELECT THIS ONE!
Xilinx	Spartan				

==========VME FPGA pin candidates ==========
========== 149 pins in the following list ==========

\CONFIG_CS1
\CONFIG_CS2
\CONFIG_PROG
\CONFIG_WRITE
\FLASH_1_CE
\FLASH_1_OE
\FLASH_1_WE
\FLASH_2_CE
\FLASH_2_OE
\FLASH_2_WE
\GA0
\GA1
\GA2
\GA3
\GA4
\VME_AS
\VME_DATA_OEB (I think this could be just pull-down + test point)
\VME_DS0
\VME_DS1
\VME_DTACK
\VME_LWORD
\VME_RESET
\VME_SYSRESET
\VME_WRITE
CONFIG_CLK
CONFIG_DONE1
CONFIG_DONE2
CONFIG_INIT1
CONFIG_INIT2
LOC_ADDR00
LOC_ADDR01
LOC_ADDR02
LOC_ADDR03
LOC_ADDR04
LOC_ADDR05
LOC_ADDR06
LOC_ADDR07
LOC_ADDR08
LOC_ADDR09
LOC_ADDR10
LOC_ADDR11
LOC_ADDR12
LOC_ADDR13
LOC_ADDR14
LOC_ADDR15
LOC_ADDR16

LOC_ADDR17
LOC_ADDR18
LOC_ADDR19
LOC_ADDR20 (required for Flash Am29LV116D)
LOC_CS_MAIN1
LOC_CS_MAIN2
LOC_CS_SLB1
LOC_CS_SLB2
LOC_CS_SLB3
LOC_CS_SLB4
LOC_CS_SLB5
LOC_CS_SLB6
LOC_DATA00
LOC_DATA01
LOC_DATA02
LOC_DATA03
LOC_DATA04
LOC_DATA05
LOC_DATA06
LOC_DATA07
LOC_DATA08
LOC_DATA09
LOC_DATA10
LOC_DATA11
LOC_DATA12
LOC_DATA13
LOC_DATA14
LOC_DATA15 (up to 15 required by SLBs)
LOC_DATA16
LOC_DATA17
LOC_DATA18 (very useful for spy fifos etc)
LOC_R/W
SCL
SDA
VME_A01
VME_A02
VME_A03
VME_A04
VME_A05
VME_A06
VME_A07
VME_A08
VME_A09
VME_A10
VME_A11
VME_A12
VME_A13
VME_A14
VME_A15
VME_A16
VME_A17
VME_A18
VME_A19
VME_A20
VME_A21
VME_A22
VME_A23
VME_AM0
VME_AM1
VME_AM2
VME_AM3

VME_AM4
VME_AM5
VME_DATA_DIR_B
VME_DATA00
VME_DATA01
VME_DATA02
VME_DATA03
VME_DATA04
VME_DATA05
VME_DATA06
VME_DATA07
VME_DATA08
VME_DATA09
VME_DATA10
VME_DATA11
VME_DATA12
VME_DATA13
VME_DATA14
VME_DATA15
VME_DATA16
VME_DATA17
VME_DATA18
VME_DATA19
VME_DATA20
VME_DATA21
VME_DATA22
VME_DATA23
VME_DATA24 (serial test points + jumper)
VME_DATA25 (serial test points + jumper)
VME_DATA26 (serial test points + jumper)
VME_DATA27 (serial test points + jumper)
VME_DATA28 (serial test points + jumper)
VME_DATA29 (serial test points + jumper)
VME_DATA30 (serial test points + jumper)
VME_DATA31 (serial test points + jumper)
VME_FPGA_CLK40
VME_LED1
VME_LED2
VME_TP1
VME_TP2
VME_SW1
VME_SW2

========== special pins (verify that they are not counted as user i/o) ==========

VME_TCK
VME_TDI
VME_TDO
VME_TMS
NCONFIG_1
NSTATUS_1
CONF_DONE_1
EPC_CLK_1
EPC_DATA_1

========== removed lines (compared to HTRproto) ==========
\FLASH_RESET (overwrite instead)
BASE0 BASE1 BASE2 (unused in HTRproto) CLOCK_SELECT (from on-board switch)
\VME_BERR (just pull-down on the board) VME_SYSCLK (can we leave it ?)
VME_A24 VME_A25 VME_A26 VME_A27 VME_A28 VME_A29 VME_A30 VME_A31
LOC_DATA19 LOC_DATA20 LOC_DATA21 LOC_DATA22 LOC_DATA23 LOC_DATA24

\VME_MODE_SELECT0, 1 , 2
\LOC_ADDR_OE (no more transition board) \LOC_DATA_OE (no more transition board)

Put test points on the unused pins, including CLOCK2 (This pin can only be used as input or clock only).

==========Programming Altera and Xilinx with JTAG==========
shouxiang wu wrote:
>
> There should be no problem. You download Altera chip with Altera software and you download Xilinx chip with
> Xilinx software. With an adapter cable, you can use Altera byteblaster as Xilinx parallel cable.

5. POWER CONSUMPTION ESTIMATE

Component	**P_{diss} x (# of components)**	**@ V**	**Source**
Dual Opt. Receivers	0.5 W x 8 = 4 W	3.3V	Data Sheet
Ch. Link TX	0.1 W x 2 = 0.2 W	3.3V	Data Sheet
SLB 3.3V [Vitesse=3W, 2 x Altera = 2 x 1W]	5 W x 6 = 30 W	3.3V	Data Sheets
Xilinx XC2V3000bf957-4	0.1 W x 2 = 0.2 W	3.3V	XPower (41 MHz,50% activity rate)
other	1W	3.3V	
Total from 3.3V	≈36 W		
TI TLK2501	260 mW x 16 = 4.2 W	2.5V	Data Sheet
SLB 2.5V	0.5 W	2.5V	
Xilinx XC2V3000bf957-4	0.6 W x 2 = 1.2 W	2.5V	XPower (41 MHz,50% activity rate)
Xilinx XC2V3000bf957-4	2.1 W x 2 = 4.2 W	1.5V	XPower (41 MHz,50% activity rate)
Regulator for 2.5V National Semi. LM1084	= output power ≈ 6W	+5V	
Regulator for 1.5V National Semi. LM1084	> output power ≈ 4.2W	+5V	
Total from 5V	≈ 25W		

Maximum front (VMEbus) 9U module power dissipation = 110W
Note: Each VME64x module has 6 +5V pins, 1 +5VSTDBY pin, 3 VPC (+5V) pins, 10 +3.3V pins, ... The pin power-rating curve given in VME64 allows approximately 1.5A per pin at 20°C. Thus each board has potentially 15A at +5V (75W), 15A at 3.3V (49.5W), ... The maximum power values ... are derived from acceptable power densities in the specified cooling environment. [see "TECHNICAL SPECIFICATION FOR SUBRACKS FOR LHC EXPERIMENTS" availab. on: http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/documents/Crate_Technical_Specification_final.pdf]

6. COST ESTIMATE

2 8-way optical ports	2 x $ 170= $340
8 Dual LC O/E	8 x $ 100 = $800
16 TLK2501 serdes	16 x $16 = $256
2 xilinx FPGA	2 x $472 = $944 or 2 x $743 = $1486
6 SLB mezzanine cards	6 x $250 = $1500
1 TTCrx & mezzanine	$ 200
Other parts (Altera,buffers, connectors)	$ 270
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Total parts	$ 4150 or $ 4700
PCB manufacturing	$ 300
Assembly	$ 250
HTR TOTAL	$ 4860 or $ 5400