CMS Trigger/DAQ

HCAL FERU System

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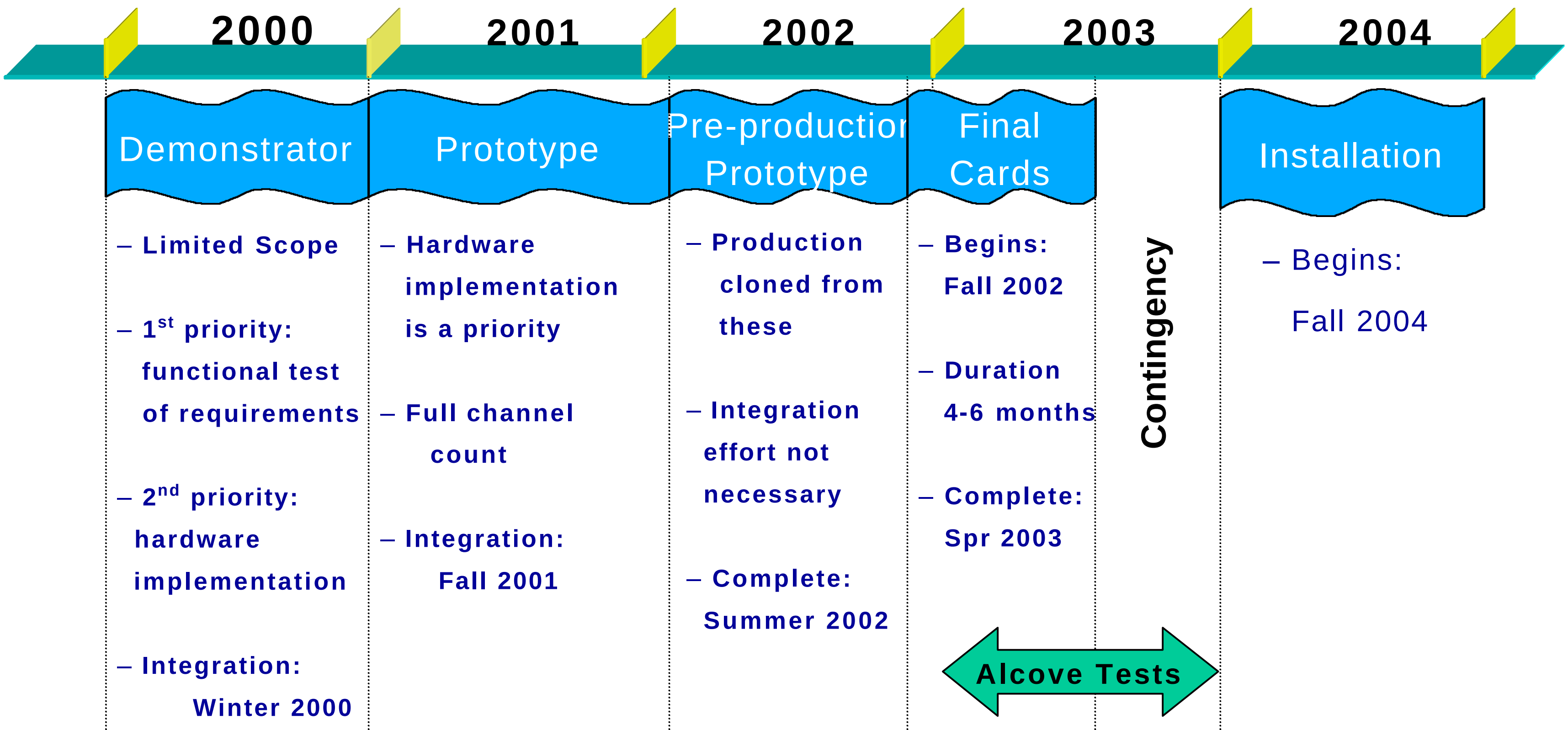
Overall Project Timelines

- Honest assessment:
  - About 3 months behind schedule.
    - Expected to start integration in Sept, won’t be until Dec
    - Plan to stick to Prototype and beyond schedule
  - Mostly due to Dzero hardware schedule slipping.



Review of HCAL Parameters

PLEASE NOTIFY OF CHANGES!!!!

- QIE Readout
  - 2 Channels per fiber
  - HP G-links
- HCAL Channels
  - Total: 4248 Towers, 463 HTR cards, 11 VME crates (as of Lehman)
- Trigger Primitives
  - Level 1 → Combine front/back HCAL towers into 1 Trigger Tower
  - 53° Overlap region under study for how to combine
- Data rates estimated using 15% occupancy at L=10^{34}

Region	Towers	Fibers	Trigger Towers
Barrel	4,968	2,304	2,304
Outer	2,280	1,140	0
Endcap	3,672	1,836	1,728
Forward	2,412	1,206	216
Total	**13,332**	**6,486**	**4,248**

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System Specifications

NEED SIMULATION CONFIRMATION

- Parameters
  - 15% occupancy at high luminosity (10^{34})
  - 10 time buckets per Level 2 Sum
  - 18 HTR cards per VME crate
  - 24 VME crates total HCAL system
  - 100 kHz average L1A rate

Amount of Data (kBytes)

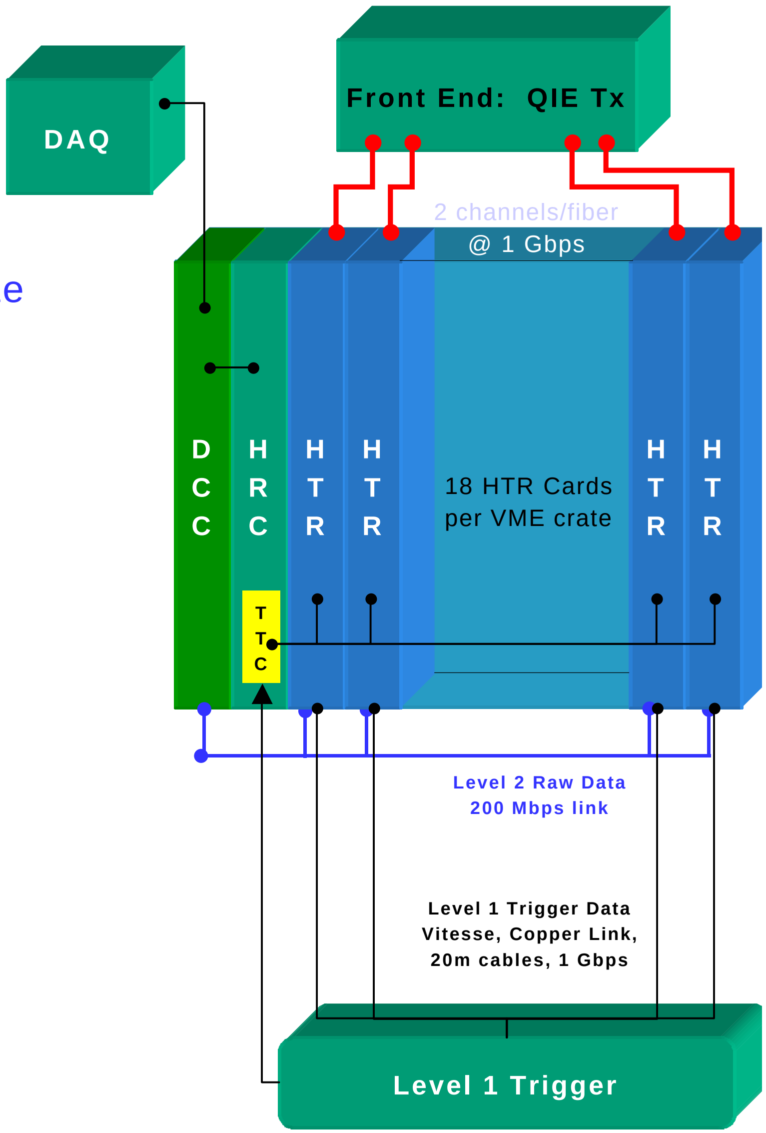
	15%	Occupancy	100%
CRATE	**2**		**14**
HCAL Total	**48**		**336**

Total DAQ Data Rate
@ 100 kHz L1A rate (GByte/sec)

	15%	Occupancy	100%
CRATE (DCC)	**0.2**		**1.4**
HCAL Total	**4.8**		**116**

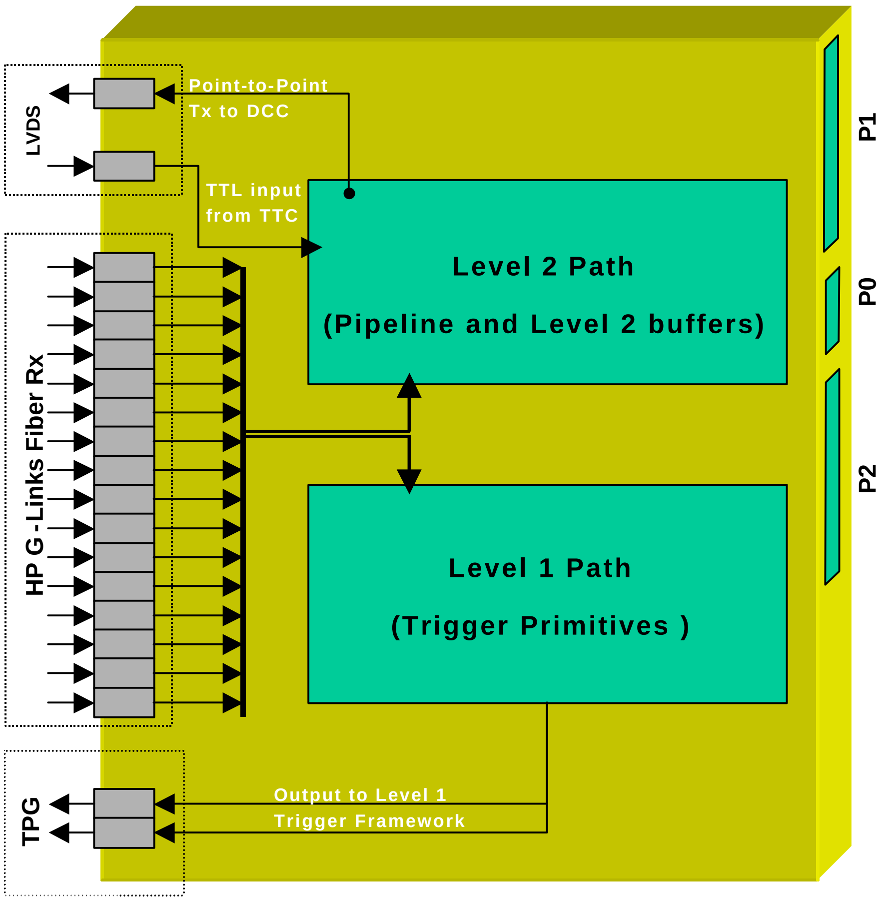
Readout Crate Overview

- 9U VIPA
  - No P3 backplanes and aux cards (saves $)
- TPG/receiver/pipeline cards:
  - 18 **H**CAL **T**rigger and **R**eadout (HTR) Cards per crate
    - Raw data fiber input
      - » 16 fibers, 2 channels per fiber=32 channels per card
    - Level 1 Trigger Primitives output
    - Level 2 Data output to DCC (next bullet)
- Data Concentrator:
  - 1 DCC card (**D**ata **C**oncentrator **C**ard) per crate
    - Receives and buffers L1 accepts for output to L2/DAQ
- Crate controller:
  - 1 HRC card (**H**CAL **R**eadout **C**ontrol Module)
    - VME
    - CPU for slow monitoring
    - FPGA logic for fast monitoring
    - TTC signal fanout (ala ECAL)



HCAL TRIGGER and READOUT Card

- All I/O on front panel
  - TTC (via TTCrx chip):
    - Single connector running LVDS
  - Raw data Inputs:
    - 16 digital serial fibers from QIE
  - DAQ data output to DCC:
    - Single connector running LVDS
  - Level 1 TPG data outputs:
    - Vitesse
      - 8 shielded twisted pair
      - 4 per single 9-pin D connector
    - LVDS possibility?
      - May be easier to implement…

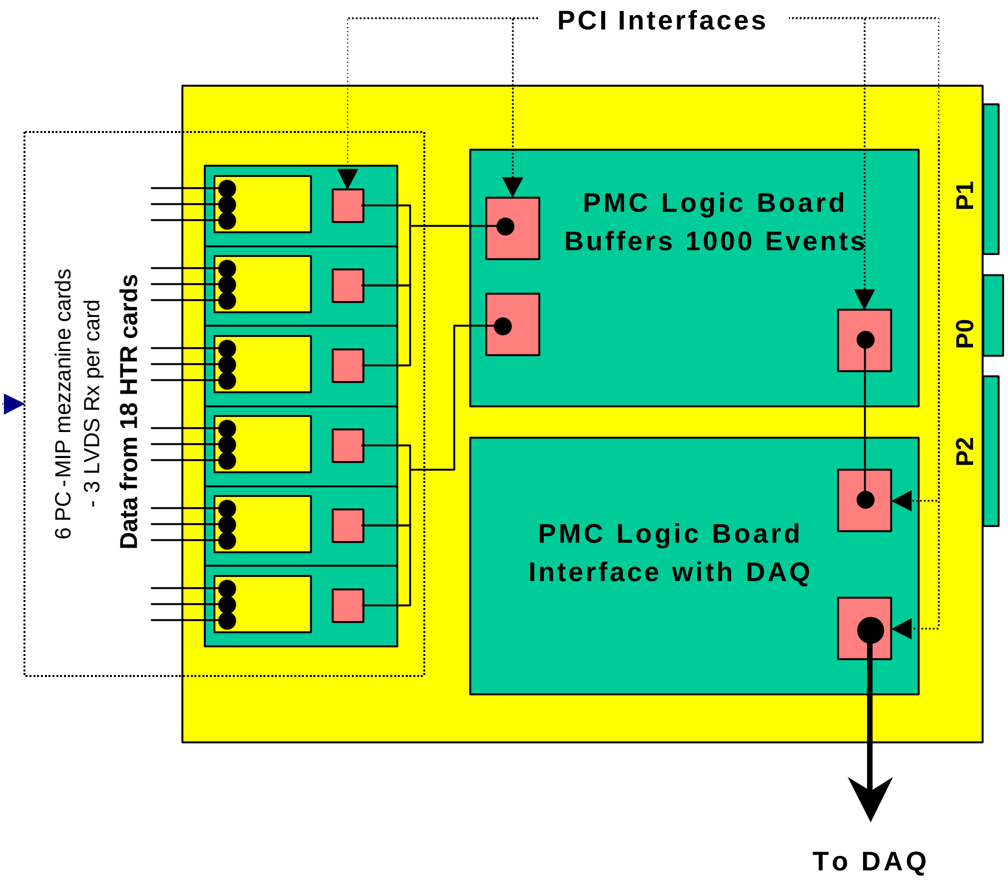


- FPGA logic implements:
  - Level 1 Path:
    - Trigger primitive preparation
    - Transmission to Level 1
  - Level 2/DAQ Path:
    - Buffering for Level 1 Decision
    - No filtering or crossing determination necessary
    - Transmission to DCC for Level 2/DAQ readout

Data Concentrator Card

Motherboard/daughterboard design:

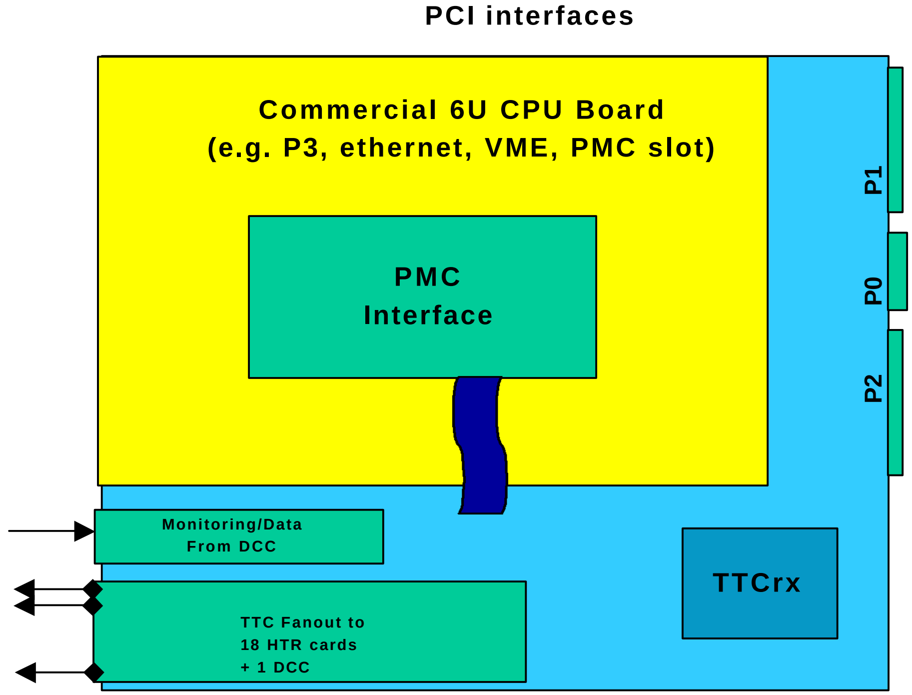
- Build motherboard to accommodate
  - PCI interfaces (to PMC and PC-MIP)
  - VME interface
- PC-MIP cards for data input
  - 3 LVDS inputs per card
  - 6 cards per DCC (= 18 inputs)
  - Engineering R&D courtesy of D∅
- 2 PMC cards for
  - Buffering:
  - Transmission to L2/DAQ via Link Tx



Hcal Readout Control Module

Commercial-based prototype design:

- Build around commerical P3 6U cpu card
  - Cheap
  - “Ubiquitous”
- Functionality:
  - Input from DCC
    - To be determined
    - Monitoring and VME data path
  - TTC fanout
    - TTCrx (chip or daughtercard)
    - Fanout to all 18 HTR cards plus DCC
  - Slower Monitoring and crate communication
    - On CPU board via PMC card
  - Monitoring: (FMU, or Fast Monitoring Unit)
    - FPGA implemented on PMC daughter board
  - Busy signal output (not shown)
    - To go to HCAL DAQ Concentrator (HDC)



HTR Overview

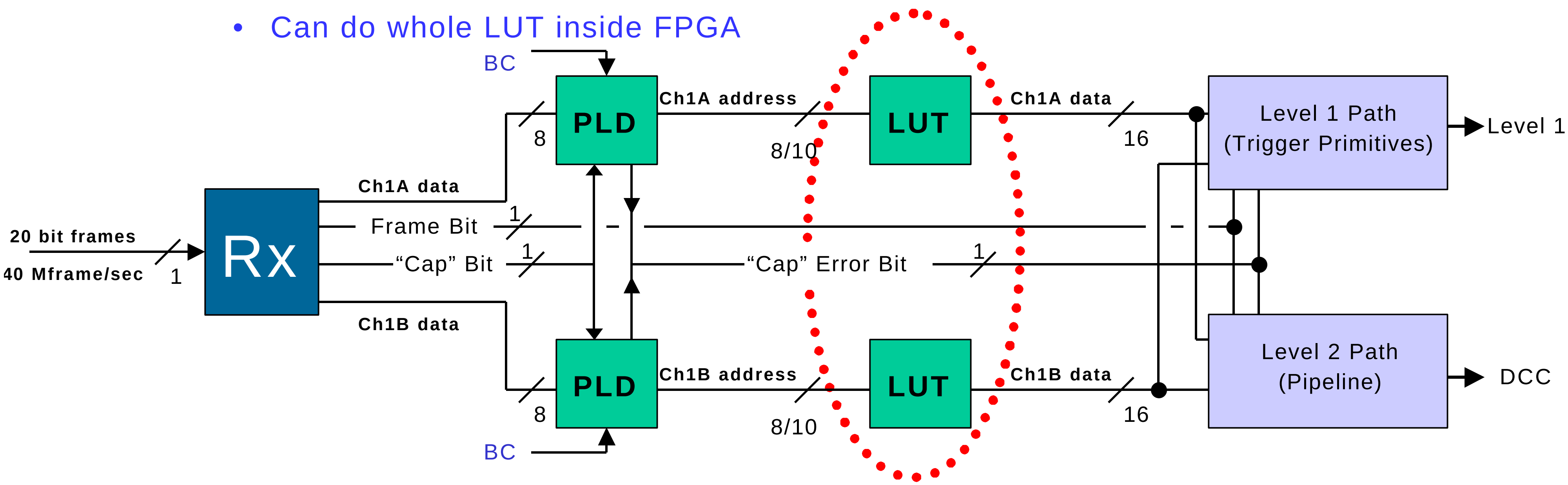
- Specs
  - 18 cards per VME crate
  - 16 fibers per card, 2 channels per fiber = 32 channels per card
- Functions
  - Digital serial input data:
    - QIE capacitor calibration
    - Linearization
    - Tx/Rx error detection
  - Level 1
    - Trigger primitive preparation
      - 1 Trigger Tower = front+back HCAL Tower sum plus Muon feature bit for MIP consistency
    - Synchronized transmission to Level 1
  - Level 2/DAQ
    - Buffering for Level 1 Decision
    - Filtering
      - Optimize resolution and associate energy with crossing
    - Transmission to DCC for Level 2/DAQ readout

HTR Card Conceptual Design

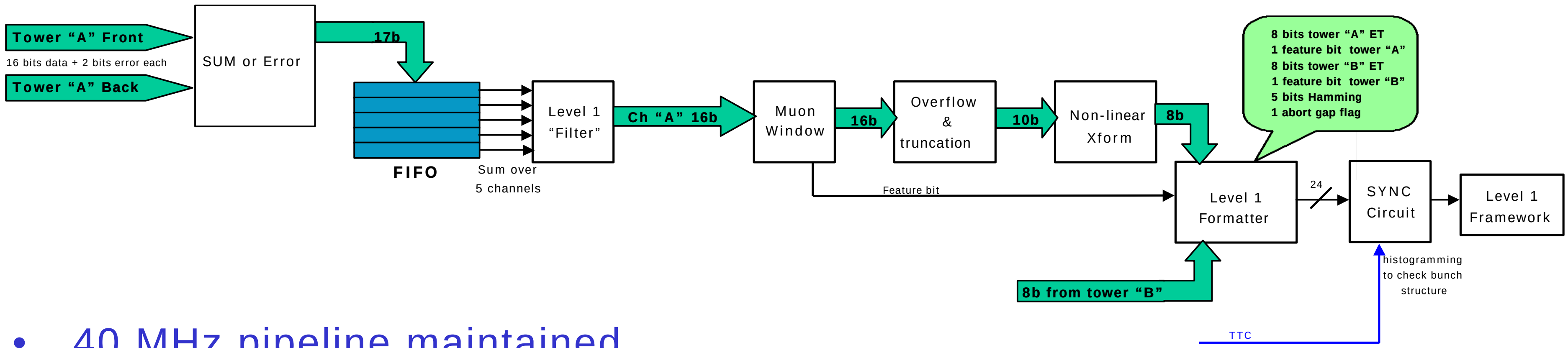
- Current R&D design focusing on
  - Understanding requirements
    - Interface with FNAL and CERN people
      - Carlos da Silva has turned Tullio Grassi into *THE* US TTC expert!
  - Minimizing internal data movement
  - Large (and fewer) *vs* Moderate (and more plentiful) FPGAs
    - Altera APEX 20k400 for the demonstrator…
  - No card-to-card communication
    - Has implications with respect to summing in 53° region, and fiber routing
- Demonstrator R&D has begun
  - Will demonstrate functionality but not actual implementation
    - 25% of data inputs (4 fibers, 8 channels)
    - I/O on front panel
    - Full TTC, Level 1 Tx and DCC Tx
    - 6U VME
    - FPGA VHDL for LPD functions and PLD for synch chip
  - This will allow us to be sure we can design the 9U full 32 channel card

HTR Schematic

- Lookup table (LUT)
  - Input: QIE 8 bit floating plus 2 bits "cap"
  - Output: 16 bit transverse energy
  - Implementation:
    - 256 addresses X 16 bit data = 4k bits/channel
      - X 32 channels = ~128k bits/card
    - Remaining 2 bits (cap calibration) via FPGA algorithm
    - Can do whole LUT inside FPGA



Level 1 Path



- 40 MHz pipeline maintained
- Trigger Primitives
  - 8 bit "floating point" E to 16 bit linear E_T
  - Combination of HCAL towers into TRIGGER Towers
    - Barrel, Forward, Endcap: 1 TT = Front+Back Dept for single HCAL tower
    - 53° transition region under study
    - Rad damage region η=2.5→3 add 4 depths
  - Muon MIP window applied, feature bit presented to Level 1
  - Relevant TTC signals from HRC card
  - Level 1 Filtering using simple algorithm and BCID and Monte Carlo guides

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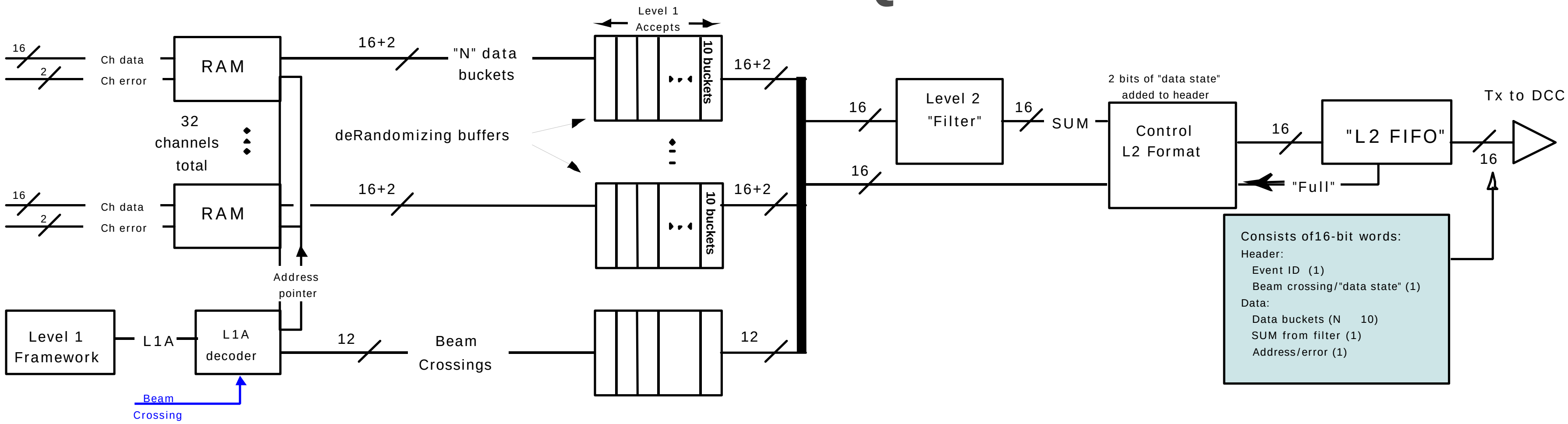
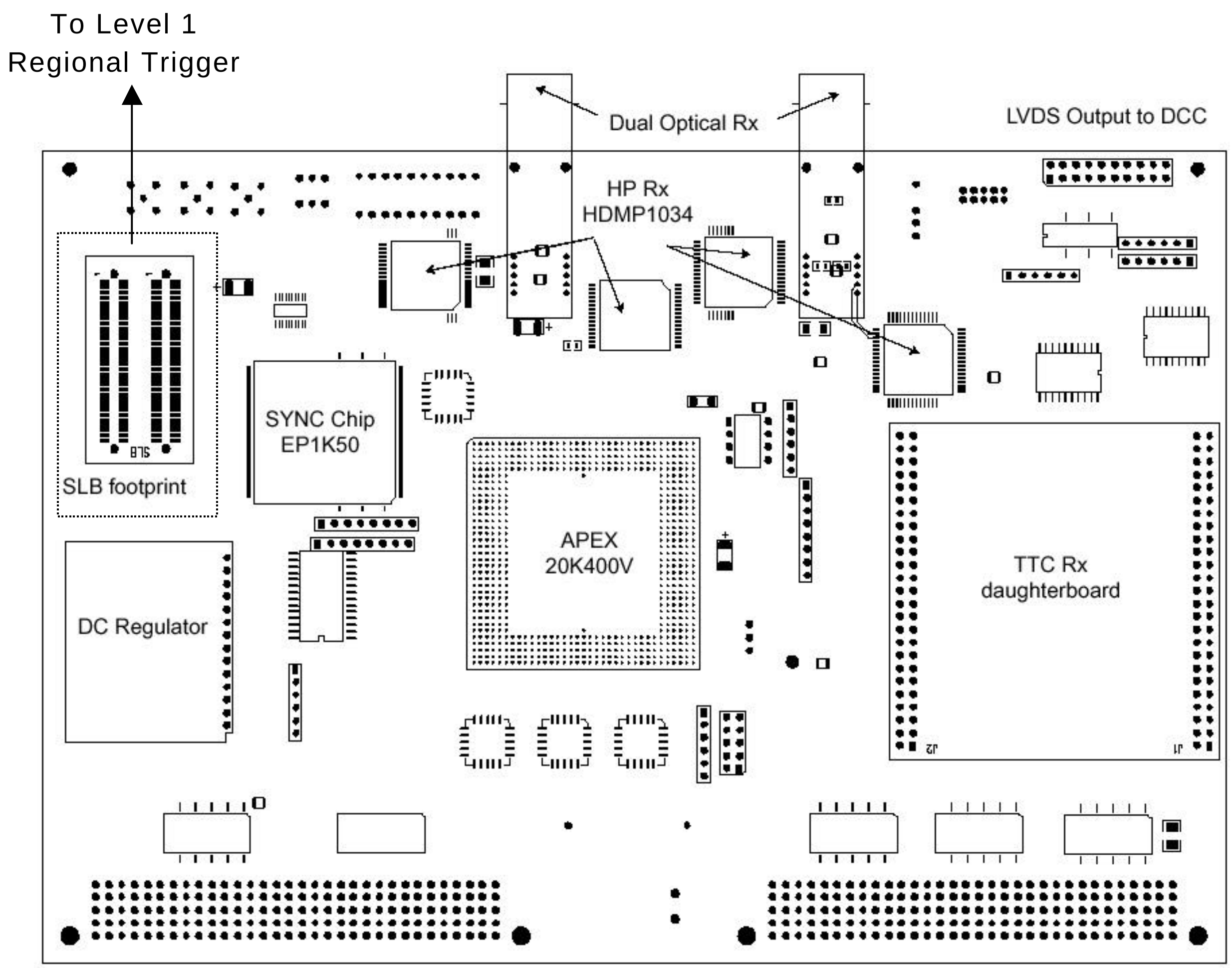
Level 2/DAQ Path



- 40 MHz pipeline into RAM, wait for L1 decision
  - 18 bits wide X 5μsec buffer = 3.6k bits/channel
  - 32 channels per card = 115k bits
- Level 1 Accept causes time slices clocked into derandomizing buffers
  - Assume 10 time buckets
  - Apply HCAL proposed trigger rule: no more than 22 L1A per orbit
    - Deadtime < 0.1% given 100 kHz L1A
  - Accommodate 44 buffers: 10 x 18 x 44 = 8k bit/channel
  - 32 channels per card = 253k bits

HTR Demonstrator Design

- Consists of:
  - 6U VME board
  - Dual Optical Rx (4 fibers)
  - HP deserializer chips
  - TTCrx daughterboard
  - APEX 20k400
    - Has enough memory
  - LVDS output to DCC
  - SLB footprint for TPG output
- Schedule:
  - Layout complete
    - Verification process
  - Will route and send out by next week (10/16)
  - Expect to have boards by late Oct or early Nov



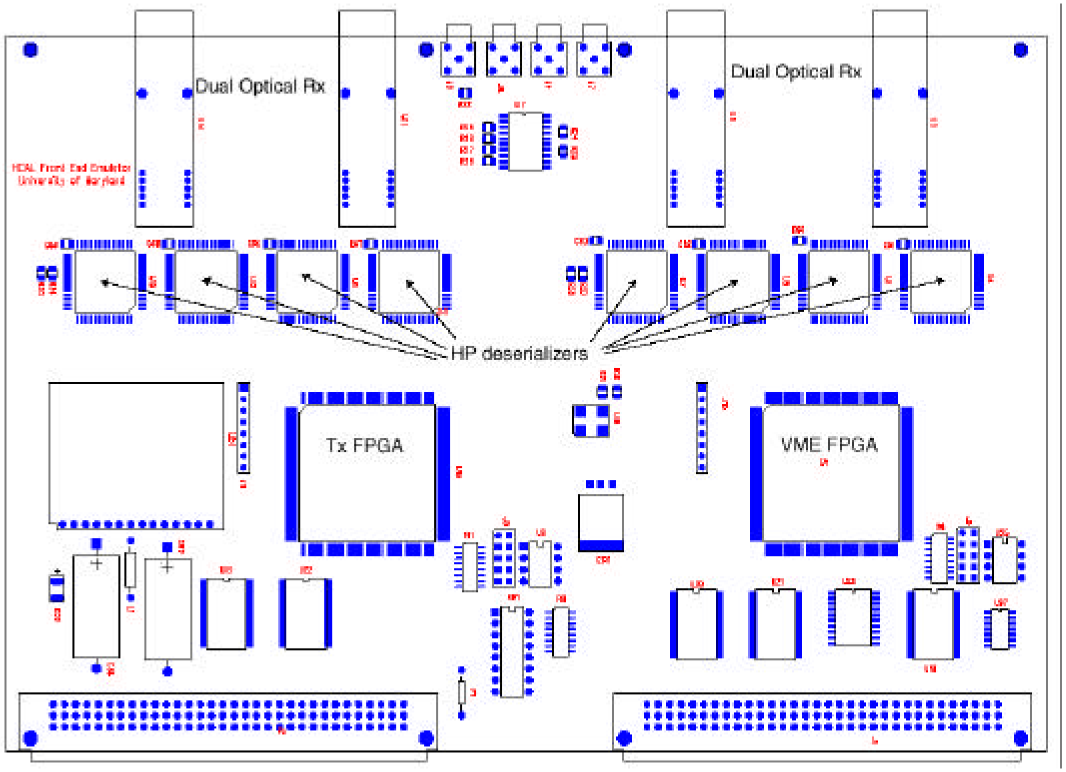
HTR Demonstrator Costs

- Parts: $2.5k/board
  - APEX 20k400 (1) $1050
    - Expected to be ~$400 in a few years
  - Optical receivers (2) $ 300
  - Deserializers (4) $ 400
  - Configuration EPROMS (4) $ 120
  - 1k50 for Synch Chip (1) $ 50
  - TTCrx (1) $ 150
  - SLB (1) $ 150?
  - Miscellaneous (drivers, connectors, etc) $ 200
- Boards: $500/board (8 layer 6U) + $1200 setup costs
- Assembly: $200/board + $700 setup
- Total:
  - $2k setup + $3.2k/board = $18k for 5 boards
  - Additional boards would be at the $3.2k level
  - Lehman estimate: $3k/board (forgot setup charges), 5 boards, $15k

6U VME “Fiber” Boards

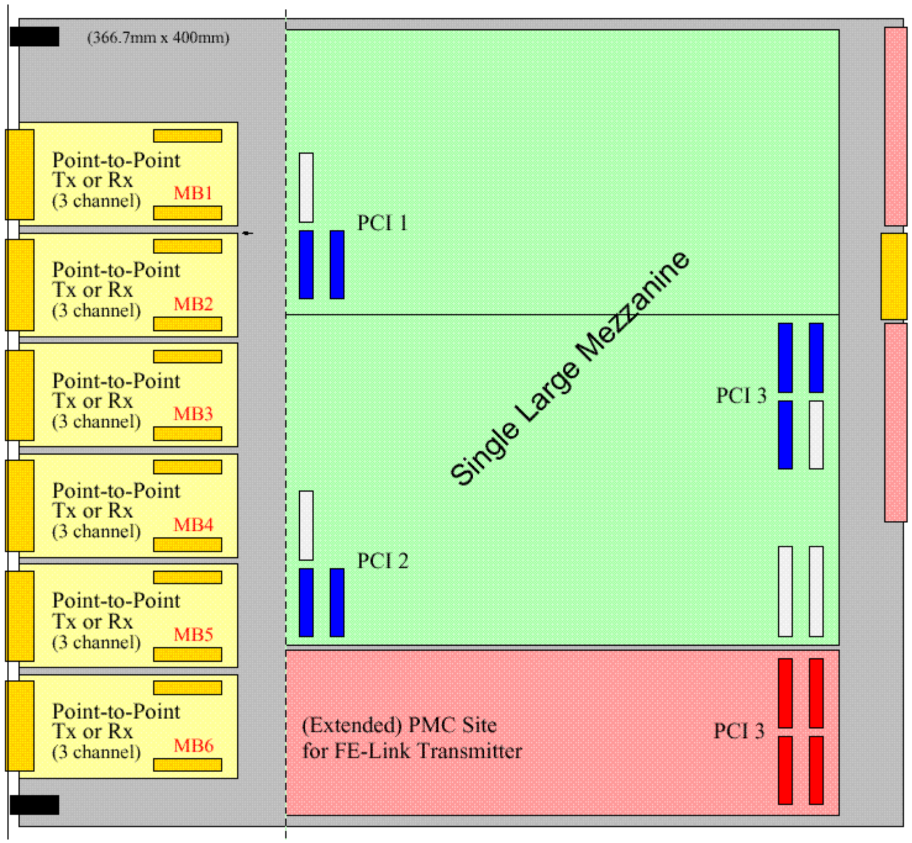
- HP tester
  - Being tested and debugged
  - Contains 1 Tx and 1 Rx
    - Optical and deserializer
  - Learn how the optical/ deserialization chips work
- Transmitter board (FEE)
  - 8 Fiber outputs (was 4 for Lehmann)
  - VME interface
  - FPGA programmable
  - This will be our data source for integration tests.
  - Layout complete, ready for fabrication (~3 weeks)
  - Costs
    - $2.5k/board Lehman, build 5
    - Transmitters (4) $1.2k
    - Total about $3.7k/board

Transmitter (FEE) Board



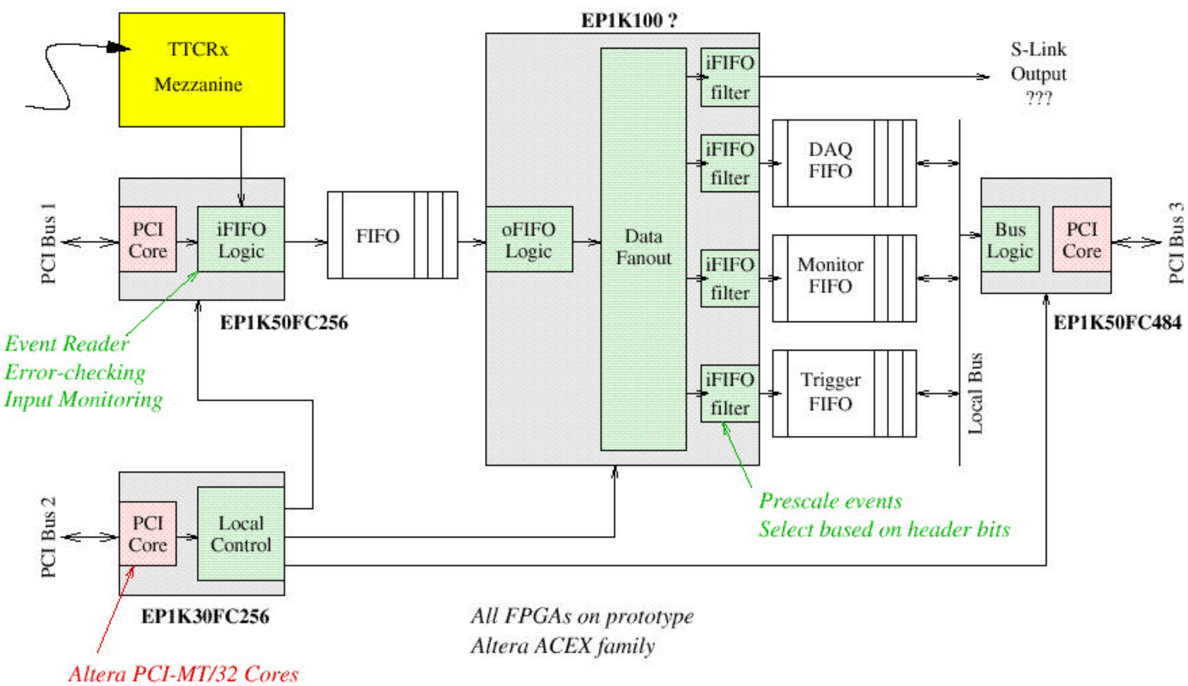
DCC

- TTCrx
- PC-MIP cards for data input
  - 6 cards, 3 LVDS Channel Links per card
- PMC cards for functionality
  - DDU
    - Buffers for DAQ
    - Processing FPGA
    - Dual Port Memory
    - Protocol FPGA
  - RUI Link Tx
- Build motherboard to accommodate
  - PCI interfaces
  - VME interface



DCC Logic Layout

- TTCrx (chip)
  - Event # and L1A each event
- Data from 18 HTR buffered in iFIFO
  - dual PCI buses, 9 HTR per PCI
  - Event # match and event error checks done here
- Large FPGA reads events from FIFO
  - distributes to 4 streams (all with FIFO-like interfaces).
    - First output is to DAQ via S-Link
    - Other three are all identical large FIFOs which may be read from VME via PCI.
  - Each stream can prescale events and/or select by header bits.
- Local control FPGA provides independent access via VME/PCI for control/monitoring while running.



DCC Demonstrator Functions

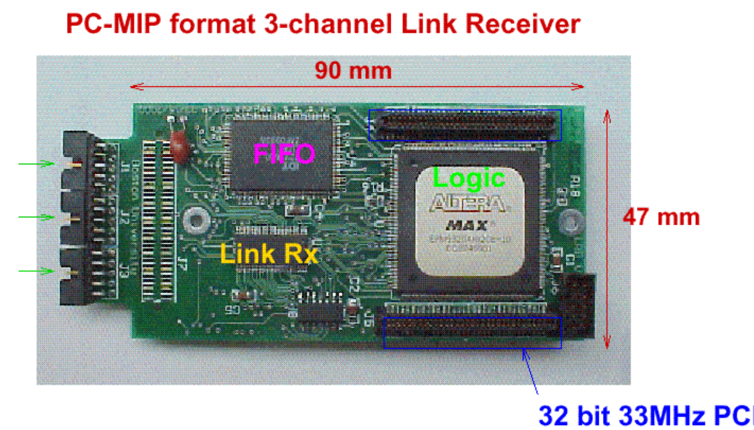
- Event building from up to 9 HTRs
  - Automatic event building across PCI bus by receiver logic
  - Event # checking
  - Controlled by TTC L1A
  - Data rate 100 Mbyte/sec – PCI limited
- Event filtering to output streams
  - Prescaled for monitoring/spying
  - Preselected by header bits
- Error checking and monitoring
  - Event number check against L1A from TTC
    - Demonstration of system-wide synch capability
  - Line error monitoring
    - Built in Hamming ECC
  - Fifo occupancy monitoring

DCC Demonstrator Implementation

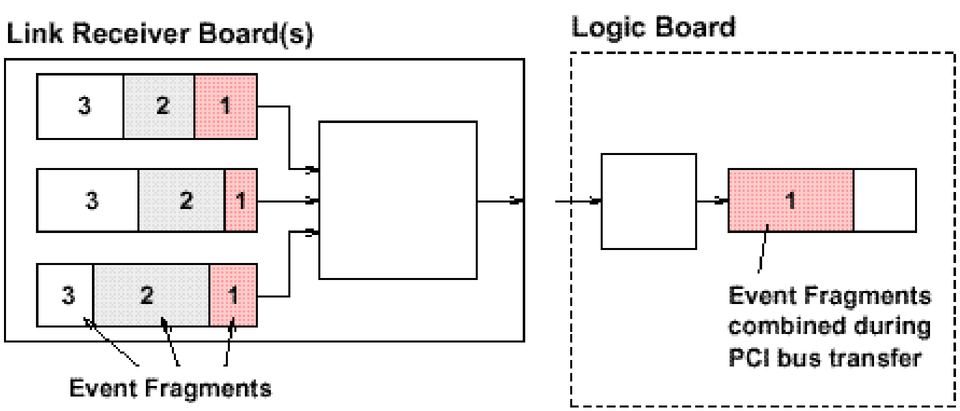
- Simplifications for rapid prototyping
  - Initially 3 HTR (can be expanded to 9)
  - No monitoring or “Trigger/DAQ” dedicated outputs
  - Simple S-link output for DAQ
  - TTCrx daughterboard
  - Use existing motherboard designs
  - FIFOs external to FPGAs
- Planned implementation
  - 3 FPGAs with Altera PCI cores and other logic as needed
  - 1 large FPGA for processing and fanout
    - Input logic
      - Reads events from FIFOs and performs error checking
    - Output logic (data driven)
      - Selects events based on prescaling or header bits
      - Writes to FIFO or FIFO-like interfaces

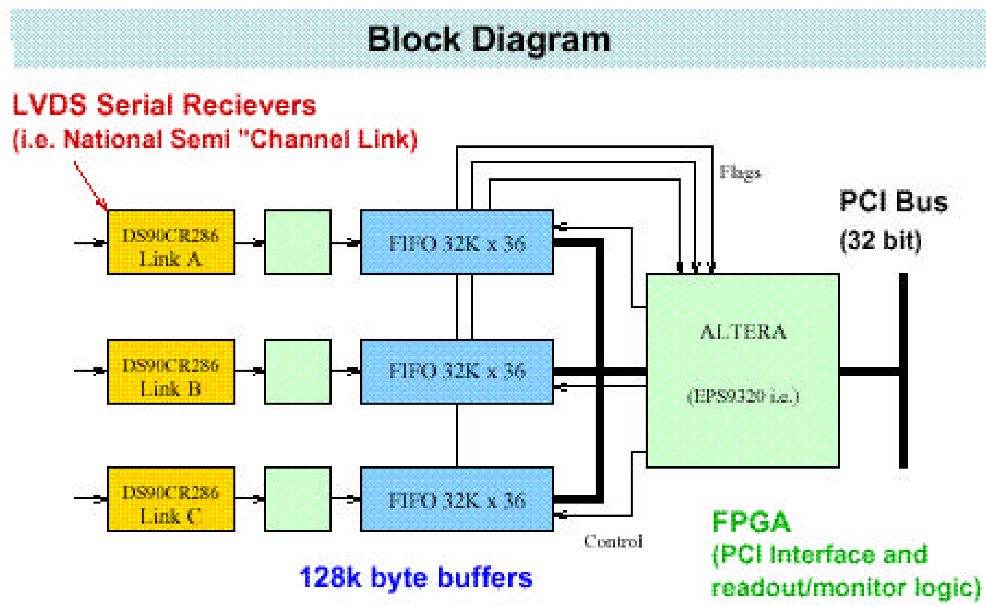
DCC PC-MIP Link Receiver Board

- Each board serves 3 HTR outputs
- LVDS/Channel Link serial receivers
- PCI bridge to logic boards
  - 2 PCI bridges
  - Each PCI bridge handles 9 HTR cards



- 33MHz x 32 bit transfer rate on link and PCI interface
- on-the-fly ECC (correct single-bit errors, detect multi-bit)
- on-board event-building, event# checking





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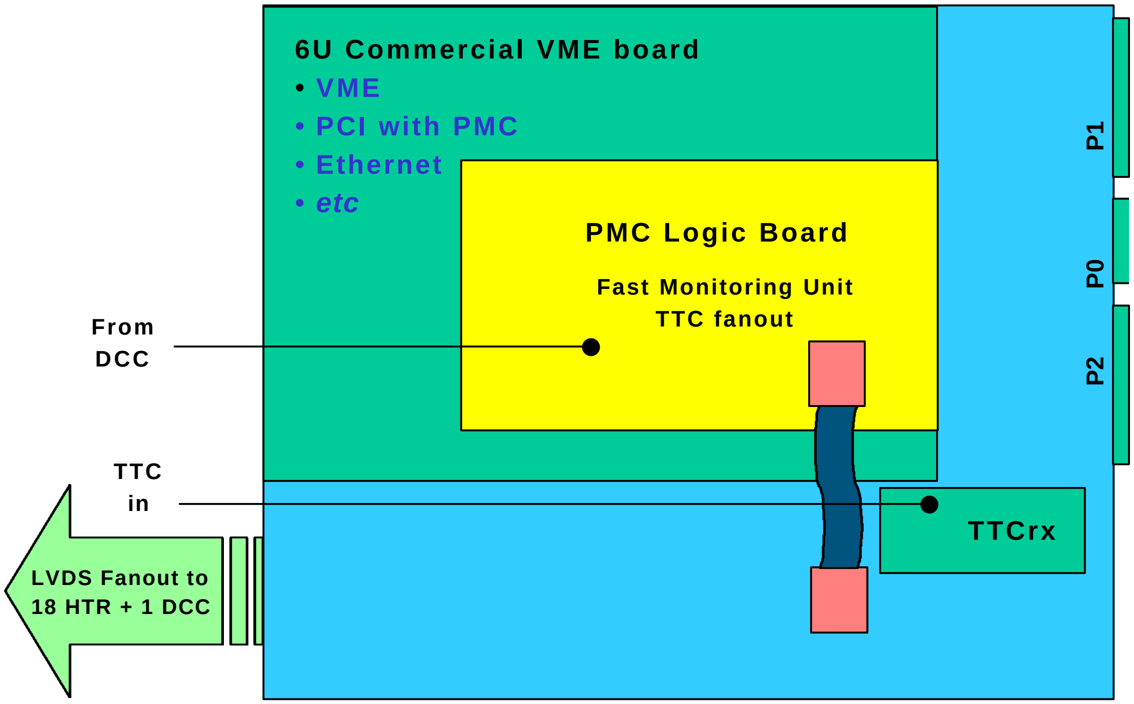
HRC

- Functionality:
  - Slower Monitoring and crate communication
  - Input from DCC
    - To be determined
    - Monitoring and VME data path
  - TTC ala ECAL/ROSE
    - LVDS Fanout to 18 HTR + DCC
  - Monitoring: (FMU)
    - FPGA implemented on PMC daughter board
  - Busy signal output (not shown)
    - To go to **H**CAL **D**AQ **C**oncentrator
- Implementation
  - Use commercial 6U cpu
  - Build rest on the surrounding frame
  - Eliminates engineering, increases up-front costs, minimizes project risk



TTC and Abort Gap considerations

- Present TTC scheme:
  - 1 TTCRx per HCAL readout crate
  - Mounted onto HRC
  - Same scheme as ECAL sends signals to DCC and all HTR cards
- Abort gap:
  - Use for monitoring
    - Laser flashes all HCAL photodetctors
    - LED flashed subset
    - Charge injection
  - Implementation issues to be worked out:
    - How to stuff monitoring data into pipeline
    - How to deal with no L1A for abort gap time buckets
    - *etc.*

Schedule

- HTR
  - March 2000: G-Links tester board (still a few bugs to fix)
    - 1 Tx, 1 Rx, FIFO, DAC…
  - August 2000: 8-channel G-links transmitter board
    - 8 fiber outputs, FPGA programmable, VME
  - November 2000: Demonstrator ready for testing/integration
    - 6U, 4 fibers, VME, Vitesse (or LVDS?), LVDS, TTC, DCC output, etc.
- DCC
  - May 2000: 8 Link receiver card (PC-MIP) produced
    - Basic DCC logic
  - Oct 2000: Motherboard prototype available
  - Nov 2000: DDU card (PMC) layout complete
  - Dec 2000: DDC prototype ready
- Integration
  - Begin by December 2000
    - HTR, DCC, TTC….integration
    - Goal: completed by Jan 2001

FY2001 Requirements

- Some of these costs are actually FY00 and some are FY02, depends on the schedule
  - Behind schedule, so some FY00 money spent in FY01
  - But then FY01 money would be spent in FY02
  - All in all, probably a wash….
- Totals:
  - Engineering: $250k
  - M&S: $150k

	Engineering		M&S	
	Days	Cost	Cost	Comments
Maryland	340	$163.2	$50k	$15k Demo, $15k prototype, $20k tester cards
BU	105	$44k	$40k	Half demonstrator, half prototype
UIC	127	$54k	$50k	Same as BU

UIC Engineering Issues

- WBS/Lehman request review:
  - Just shy of 2 years total
  - UIC to kick in half
- This is probably a realistic estimate
  - If UIC doesn't kick in half, then CMS will surely have to.
- Problem:
  - 2000-2002, UIC estimates ~.5 FTE engineering.
  - Difficult for UIC to hire an engineer for half-time work!

Year	Days	
1999	40	Demonstrator
2000	120	Demonstrator+Integration
2001	90	Prototype + Integration
2002	120	Prototype + Production
2003	10	Production
Total	380	

- Recommendation: CMS agree to pick up cost of the other half if Mark cannot finagle it out of the UIC Physics Dept head
  - Ultimately, we will have to do this if we cannot get UIC to pony up half.
  - We should support Mark in trying to convince the UIC Dept Head
    - But he needs to hire a GOOD engineer and get going!!!

BU Issues

- There is no physicist working on this project!
- Why do we care?
  - Because Eric is overloaded
  - Other BU faculty might resent this project and cause trouble.
  - Priority of the BU shop jobs?
  - Can we really hold Sulak accountable?
  - And so on.
- I am more and more worried about this
  - BU shop cannot be doing “mercenary work”
- Recommendation:
  - BU should have a physicist.
  - At least, a senior post-doc to work for Sulak.