HCAL
Trigger / Readout

Texas Tech Meeting

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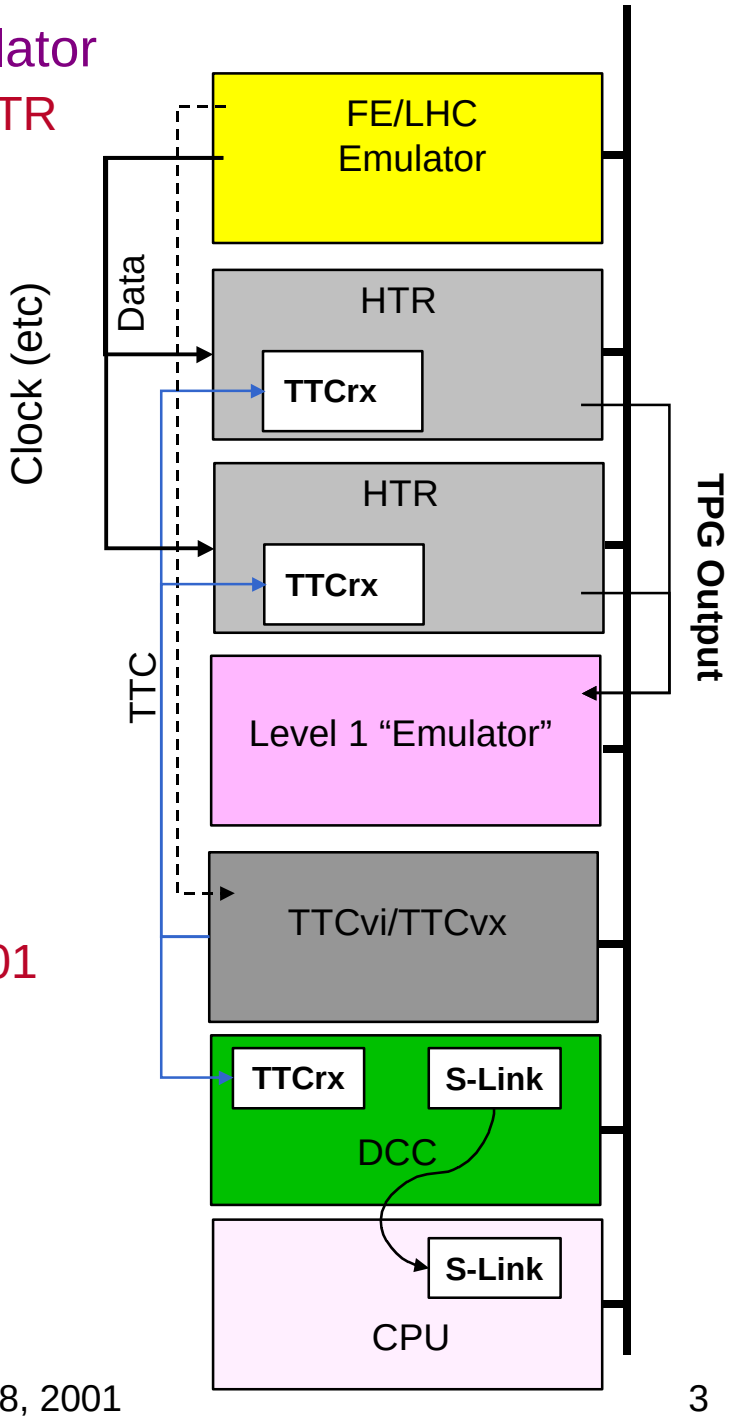
Outline

- Trigger/DAQ Demonstrator project
  - HTR demonstrator
  - Front-end Emulator
  - DCC demonstrator
  - DAQ
- Cost/Schedule

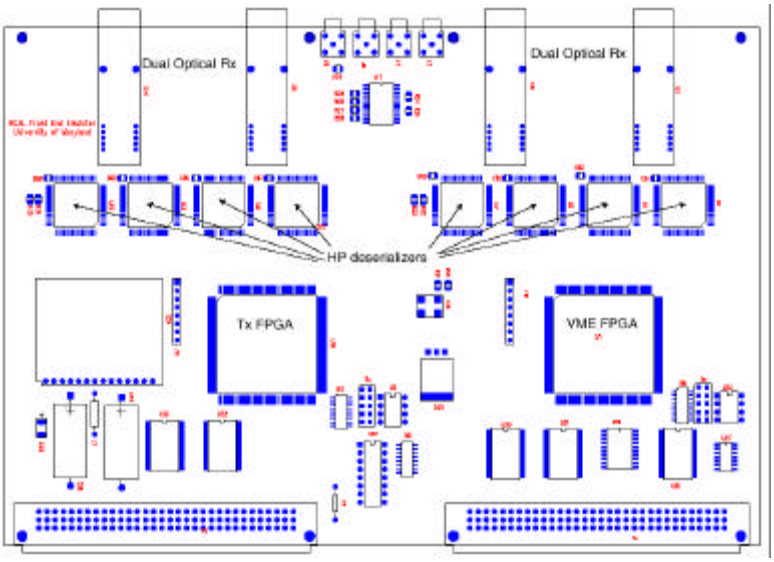
Demonstrator System Design

- Front-end and LHC emulator
  - Fiber data source for HTR
    - Uses crystal clock
  - Signals for TTC
- HTR demonstrators
  - Data inputs
  - TTCrx daughterboard
  - TPG output
- TTC system
  - TTCvi and TTXvx
- DCC demonstrator
  - Full 9U card
  - S-link output
- Level 1 “Emulator”
  - Wisc to provide Rx ~6/01
  - Carlos to provide Tx
  - HTR is ready
- Crate CPU
  - Commercial card
  - Running Linux
  - S-link input



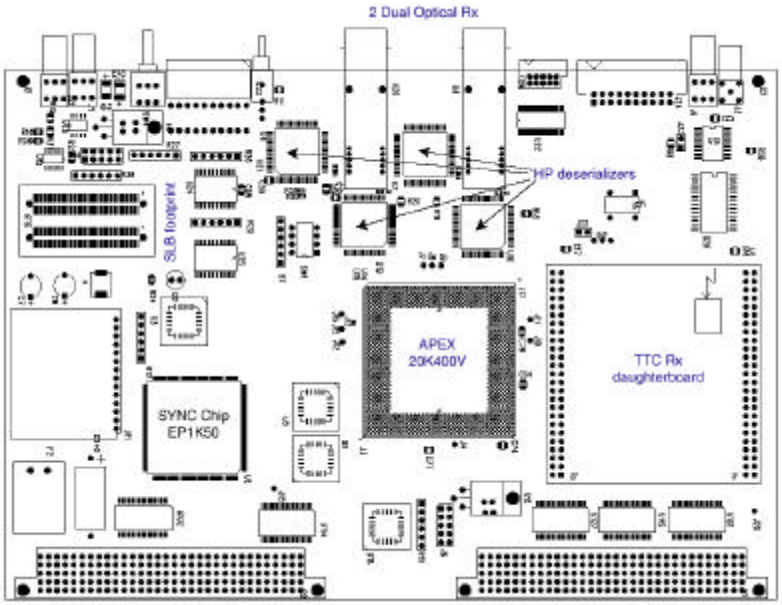
Front End / LHC Emulator

- 6U VME board
- 8 fiber data outputs simulates HCAL
- System signals:
  - Internal 40MHz crystal + FPGA (Altera 10k50)
  - Generates master clock, L1A, and BC0
  - All are ECL outputs
    - Clock, L1A, Orbit, BC0, spares
- LHC pattern generated internally
- Board is being stuffed, back in 1 week



HTR Demonstrator

- 6U VME board
- 2 Dual Optical Rx (4 fibers)
- HP deserializer chips
- TTCrx daughterboard
- APEX 20k400
  - Has enough memory
- LVDS output to DCC
- Link piggy-board footprint for TPG output
- Board is being stuffed, back in 1 week

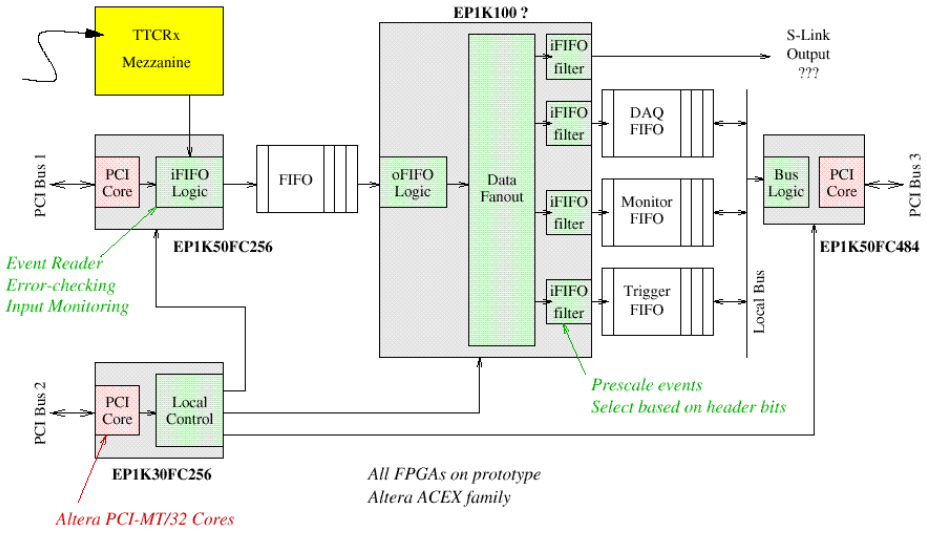


HTR / FEE FPGA Firmware

- Emulator
  - Hans Breden already working on it
  - “pretty simple” in comparison to HTR
- HTR (“LPD” etc)
  - Tullio is working on this
    - Baden to help soon as D0 stuff is finished
    - Software tools (Quartus, Synplify, Aldec, etc.)
    - Algorithm (LPD)
      - Grassi/Baden met with Magnus Hansen Jan 01
      - VHDL and knowledge changed hands
  - Simplified version soon to test I/O
  - This is a major work in progress towards a more final version

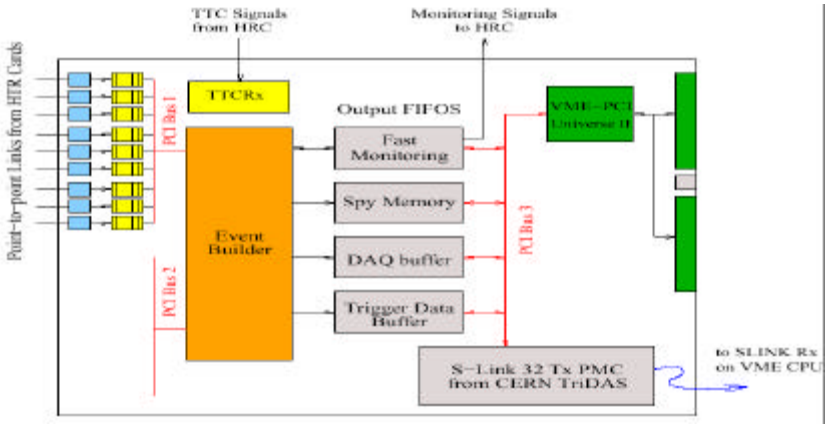
DCC Logic Layout

- TTCrx daughtercard
- Data from 18 HTR buffered in iFIFO
  - dual PCI buses, 9 HTR per PCI
- Large FPGA reads events from FIFO
  - distributes to 4 FIFO-like streams
  - Each stream can prescale events and/or select by header bits.
- Local control FPGA provides independent access via VME/PCI for control/monitoring while running.

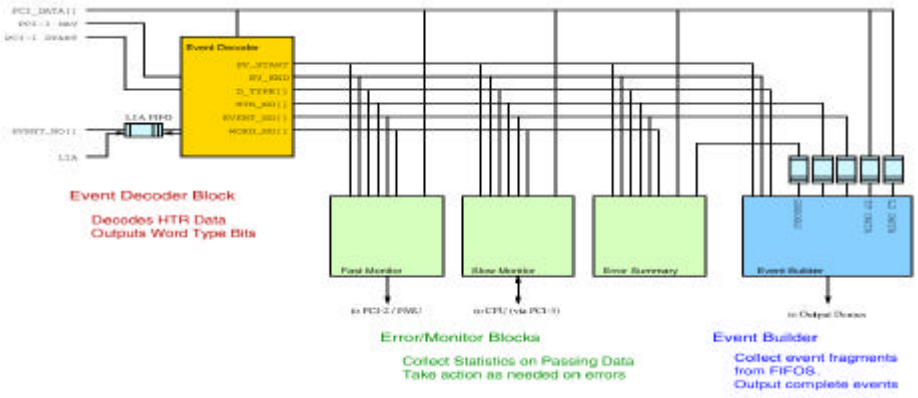


DCC Demonstrator

- DCC VME motherboard
  - 2 prototypes tested and working
  - Components for 5 for CMS on order



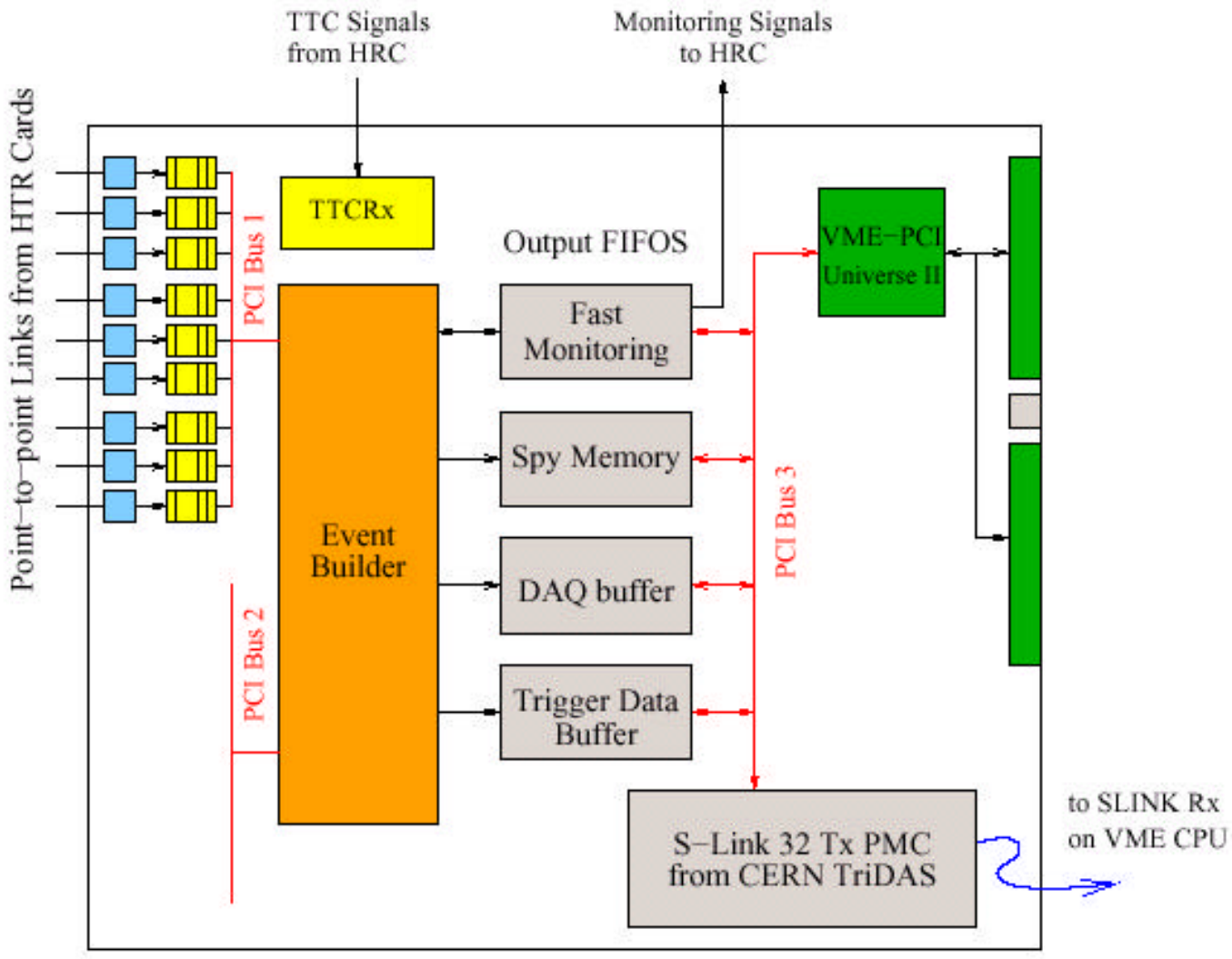
- Link Receiver Boards (input & event building)
  - 2 prototypes (2nd revision) under test
  - Components for 10 “in stock”



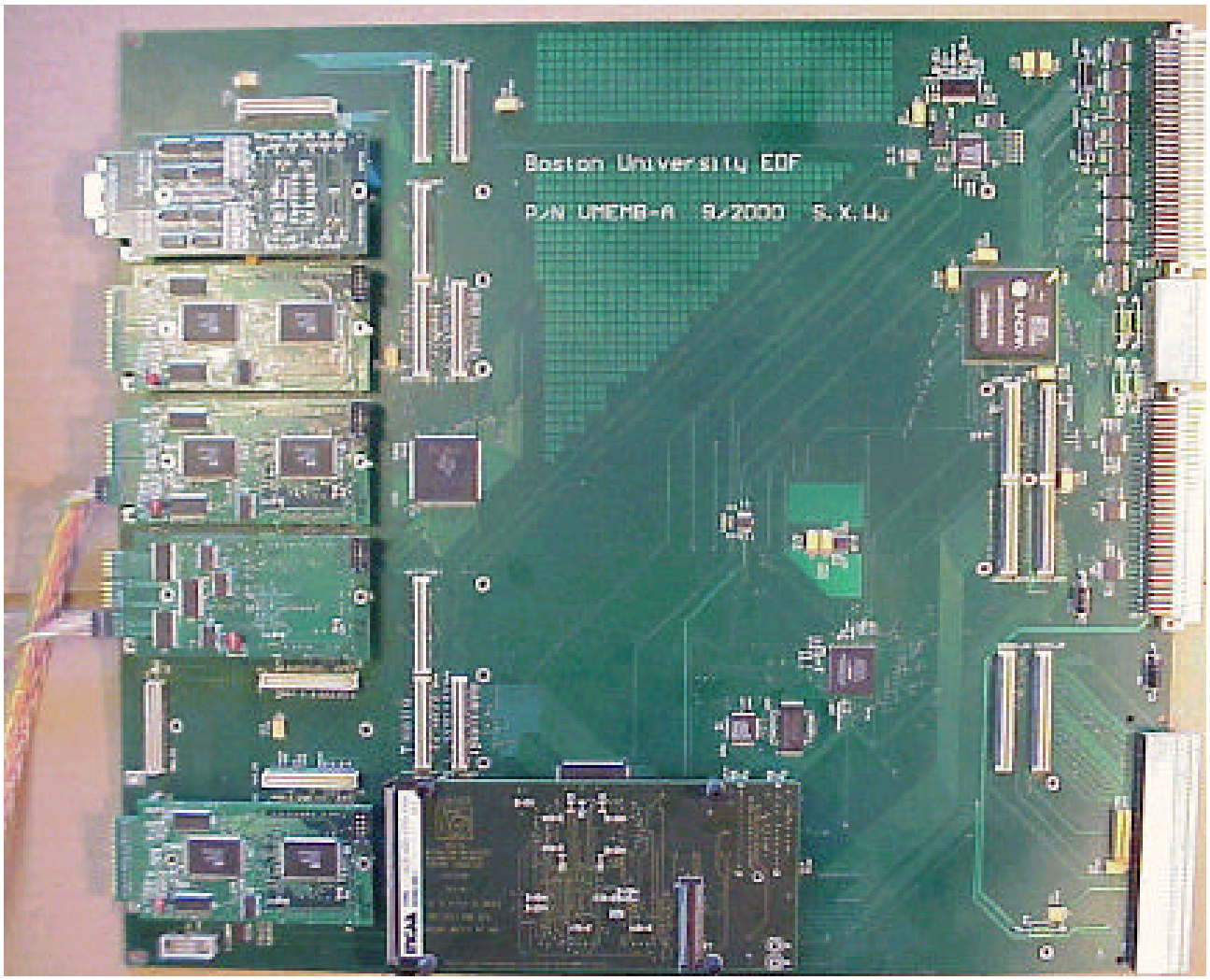
DCC Motherboard

- What's been tested so far:
  - PCI tested to 35MHz (33MHz is the PCI spec.
    - This is faster than the anticipated 28MHz
  - Burst transfers tested on PCI3
  - All PCI bridges work
  - All PC-MIP sites work
    - Used commercial digital I/O board
  - All PMC sites work
    - Used S-Link interface

DCC Overview

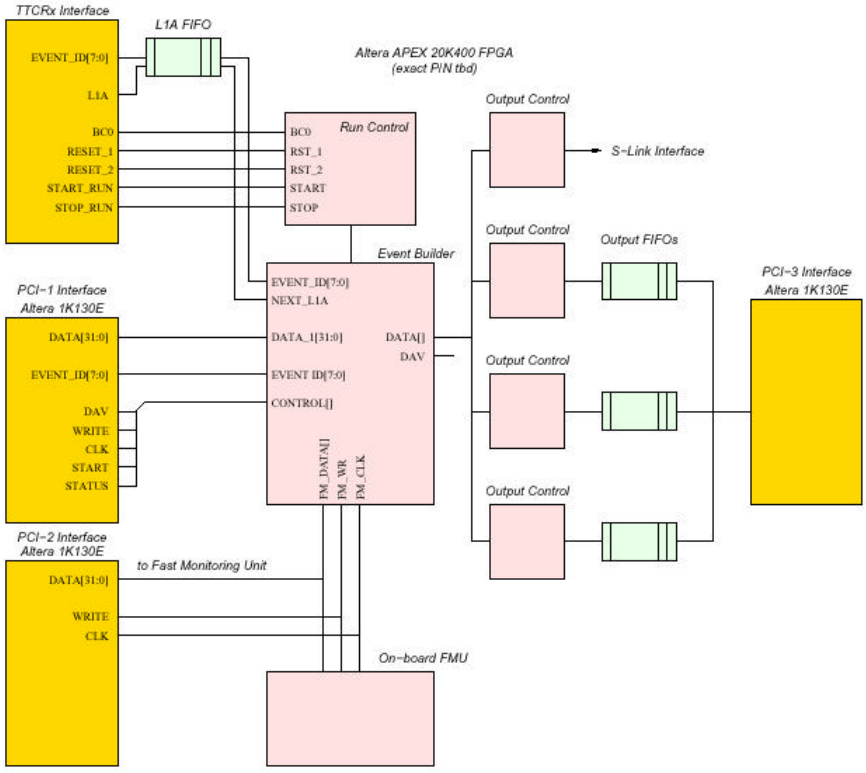


DCC Demonstrator Motherboard



DCC Demonstrator

- DCC Logic module
  - CAD Schematic done
  - PCB layout to start in 2-3 weeks
  - FPGA firmware design underway
  - Using S-link for interfaces works fine



DAQ

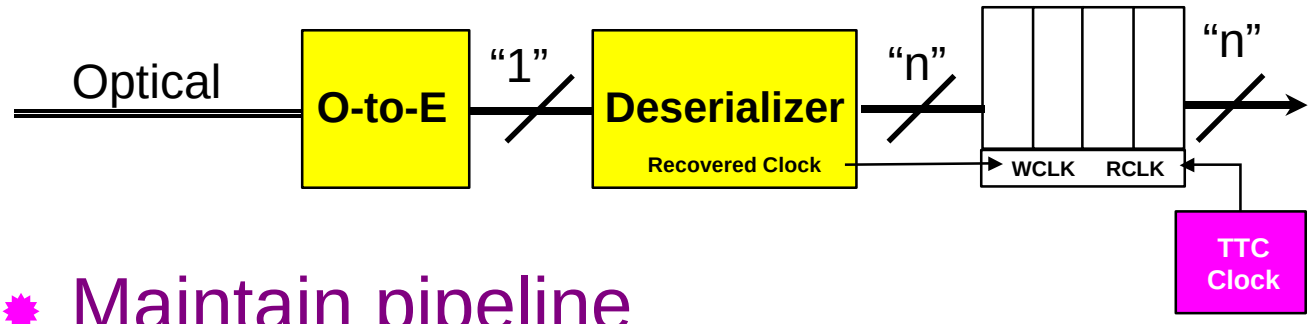
- 6U VME Pentium CPU board
  - running Linux
  - VME interface
  - Connect to TTCvi, HTR, and DCC
- Use S-Link for direct data interface with DCC
  - Will also have VME interface if needed
- UMD, BU, and UIC already purchased
  - Not necessarily have gotten Linux up yet
- Chris Tully has agreed to help
  - Students, maybe himself
- Overall integration still up in the air
  - Need to get organized on this
  - Video meeting next week to start
    - Goal: get UIC, BU, Princeton, UMD workers to be at UMD and work on this together, pound it out!

Testing Goals DAQ

- Run Demonstrator project at UMD
- Be ready to run FNAL source calibration project next summer

Testing Goals
HTR

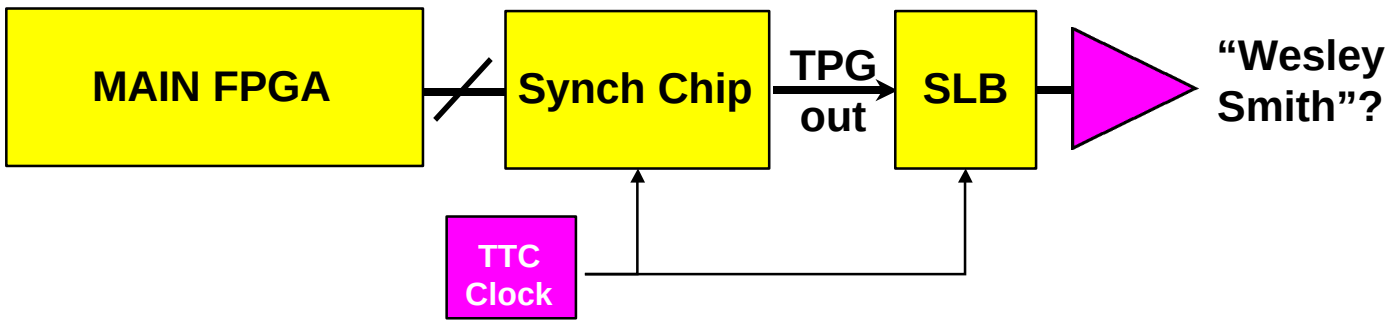
- Receiving optical data
  - G-links clock recovery
  - Asynchronous FIFO
  - TTC clock for FIFO RCLK



- Maintain pipeline
  - With error reporting
- Crossing determination
  - Send data to HTR demo coincident with selected 25ns time bucket
  - Recover this particular 25ns time bucket
  - Investigate various algorithms (with help)

Testing Goals
HTR

- Synchronization
  - All TPG data from same bucket are aligned for transmit to L1 trigger
  - Use of Synch Chip on our boards
- From L1A, verify correct data gets into DCC
  - L1A generated in the TTCvi by FE Emulator
- TPG output needs a source and a receiver!
  - Wait for Wisconsin to provide
  - Use Carlos daSilva's Link Piggy board



Testing Goals
DCC

- Input
  - Test LVDS electrical from HTR
  - Test data protocol
    - Grassi/Bard/Hazen have worked it out
  - Test (multiple) PCI interface and event building
- Buffers
  - Multiple FIFOs for various functions
    - Output to L2/DAQ (all data)
    - Monitoring (preselected)
    - Trigger verification (prescaled)
    - Other?

Testing Goals
DCC

- Error checking and monitoring
  - Event number check against L1A from TTC
    - Demonstration of system-wide synch capability
  - Line error monitoring
    - Built in Hamming ECC
  - FIFO occupancy monitoring

- DCC output
  - Use S-LINK to connect to CPU via PMC connector
    - Incurs an additional $5k expense
    - Cards already build and delivered from CERN
    - BU already tested
  - This allows us to move forward in DCC/DAQ integration ahead of schedule

Schedule

- FEE/LHC Emulator
  - Layout, fab complete, physically in board house now
  - Expect board by Feb 12
  - FPGA firmware being worked on now
    - Expect end of Feb, in time for testing
- HTR
  - Layout , fab complete, also in board house now
  - Expect board by Feb 12
  - Firmware will be an ongoing project
    - Preliminary firmware for checkout in time for testing
- DCC
  - Motherboard tested and working
  - Link receiver cards (PC-MIP) tested and working
  - PMC Logic board sometime in March or April
    - We can get started using S-Link, direct interface between DCC motherboard and CPU
    - WU is now officially full-time on this

Schedule (cont)

- Integration
  - Hardware checkout to begin this month
  - Software needs a lot of work
    - Serious efforts have to begin now on Linux DAQ etc.
    - Will begin weekly video conference meetings with
      - UMD, BU, UIC, Princeton
  - Goal:
    - Hardware and software integration to start in March
    - Be ready for FNAL source calibrations this summer
  - We are behind by 2-3 months
    - Can make some of this up by eliminating prototype stages
    - Still plan to try to stick to Lehman schedule
    - Note DCC effort is already underway, HTR is 1 week away from testing and begin of integration

Demonstrator Project Costs

- Working on reevaluation of project costs
  - Will present to Level 2 WBS mgmt soon
  - Some examples of additional Demonstrator costs:
    - HTR $3k original, $3.5k actual
    - FEE $2.5k original, $2.8k total
    - S-Link $5k
    - Additional 9U VME crate with 6U slots $5k @UMD
    - UMD CPU board $4k with software
    - Quartus requires >512M memory to run!
      - Our computer uses RDRAM!
    - Will need to clone a system for Tully
    - 2 additional DCC Motherboards ordered
    - Several additional BU startup expenses (software, etc.)
  - No difficulties expected (yet)

Overall T/DAQ Costs

- Cost savings for increasing to 3 channels/fiber
  - Can do 12 inputs for 36 channels instead of 16 inputs for 32 channels per card
- Current:
  - 463 cards
  - $2.5k/board, $480 for Rx chips
  - $1.158M total
- New:
  - 413 cards
  - $2.4k/board, $360 for RX chips
  - $0.991M total, saves almost $160k
- Realistically, this is in the continency noise but it DOES reduce the baseline

Cost Variables

- New vs Old G-Links
  - Old = 2 channels/fiber, 16 fibers/HTR
    - 20 bits x 40MHz = 800MHz
  - New = 3 channels/fiber, 12 fibers/HTR
    - 32 bits (40) x 40MHz = 1.2 (1.6) GHz
  - Advantage of New:
    - Fewer HTR (~10%)
    - Take advantage of fiber mass terminators
      - 12/connector fits nicely, use 1 per HTR
      - Significant reduction in cost of o-to-e
        - 12 vs. 16, these are expensive
      - Is it real?
- FPGA
  - Smaller is definitely cheaper
  - Critical that HCAL stick to no more than 5 channels per sum. Why?
    - Can then use 8 FPGA per HTR, 5 channels per FPGA
    - Puts constraints on fiber cabling but will help cost alot

Overall T/DAQ Costs

- Changes since baseline ($1.5M for HTR)
  - FPGA cost for Altera 20k400 TODAY (1/2001) is $1000 for single!!!!
    - Quantity in 2 years? Maybe 1/4-1/3
    - Baseline cost for FPGA: $1000
    - It might fit
  - Optical o-e
    - Baseline estimate for 2-fiber connectors $30
      - Grossly underestimated – more like $100
      - This is an $800 underestimate, which amounts to a 30% increase ($1.5M)
    - With increase to 36 channels per card, this amounts to about $200
    - Can use mass terminated fiber connectors, 12 per connector, cost is $400
      - Would bring the costs back nearer to baseline
      - Warnings from Magnus on delivery time, etc for these parts now.