USCMS HCALTriDAS

Introduction

- HCAL Front-End Readout and Trigger

- Joint effort between:
  - University of Maryland – Drew Baden (Level 3 Manager)
  - Boston University – Eric Hazen, Larry Sulak
  - University of Illinois, Chicago – Mark Adams, Rob Martin, Nikos Varelas

- Web site:
  - http://macdrew.physics.umd.edu/cms/
  - Has latest project file, spreadsheets, conceptual design report, *etc*…

- This talk:
  - Design
  - Schedule
  - Issues

CMS Inner Detector

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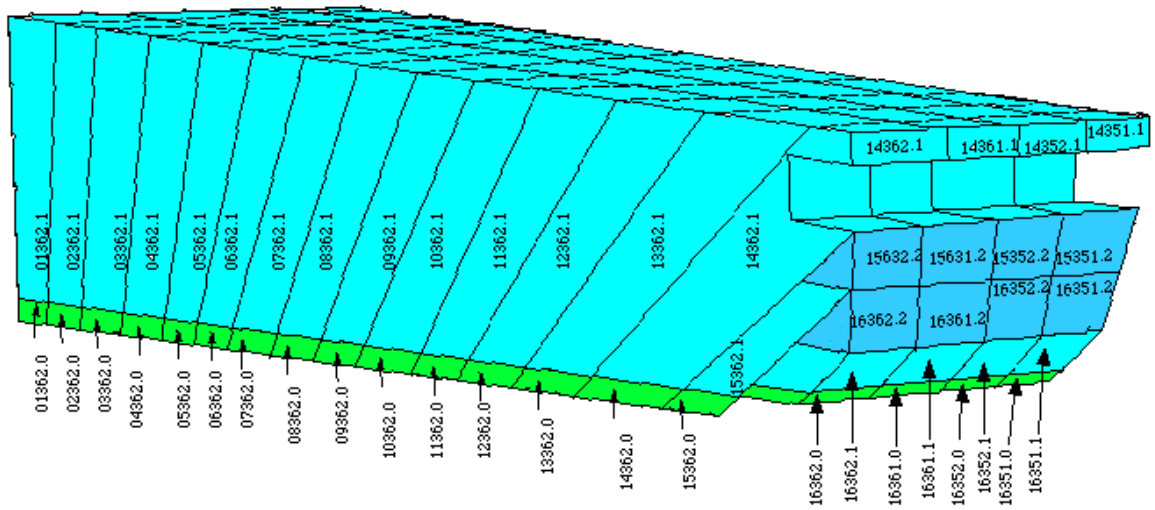
HCAL Barrel Trigger Primitives

- $0 < \eta < 1.5$
- $\Delta\eta \times \Delta\phi = .087 \times .087$
- H0 and H1 depths
- Trigger Primitive:
  - H0+H1 added together
  - TT ≡ physical tower
  - Convert to E_T via LUT
  - Muon bit added
    - 1.5 GeV < E < 2.5 GeV
    - 1 MIP ~ 2 GeV
- Level 1 data:
  - 24 bits:
    - Tower A: 9 bits:
      - » 8 bits ET nonlinear
      - » 1 bit Muon
    - Tower B: 9 bits, same as A
    - 1 Abort gap bit
    - 5 bits Hamming code



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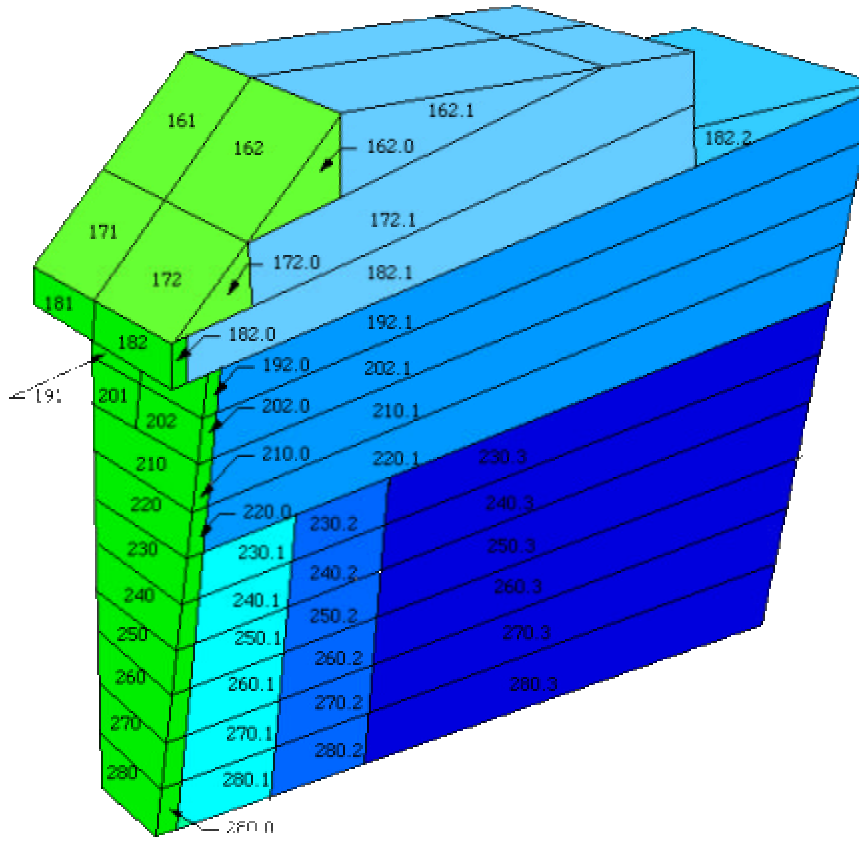
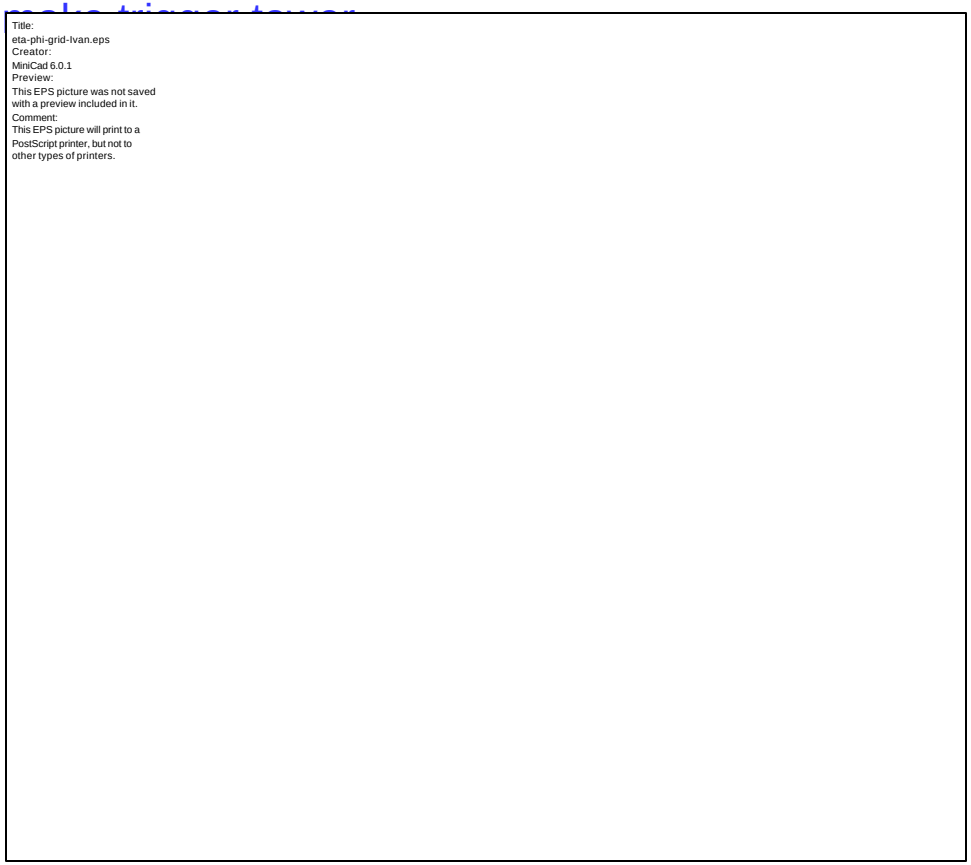
HCAL Endcap Trigger Primitives

- $1.5 < \eta < 3$
- $\Delta\eta \times \Delta\phi = .087 \times 5°$ (.087) $\eta < 1.6$
- $\Delta\eta \times \Delta\phi = .087 \times 10°$ (.175) $\eta > 1.6$
- Trigger Primitive:
  - $\eta < 1.6$
    - same as Barrel
  - $\eta > 1.6$
    - 1 TT = 2 physical towers
    - break physical tower into halves and send
- Level 1 data:
  - same as Barrel



HCAL Forward Trigger Primitives

- $3 < \eta < 5$
- $\Delta\eta$ x $\Delta\phi$ = .166 x 10° (.175)
- Trigger Primitive:
  - combine 2 in ϕ and 3 in η to make trigger tower
- Level 1 data:
  - same as Barrel



HCAL TriDAS Relevant Parameters

- These parameters drive the design and project cost:
  - HCAL Channels and topology determines
    - Total channel count
    - Total number of trigger towers (includes calibration fibers)
      - Need to understand 53° Overlap region, high rad region, fiber cabling, *etc*.
  - QIE Readout parameters determine
    - Number of channels/card
      - 2 Channels per fiber, 7 data bits + 2 cap bits per channel
      - HP G-links, 20 bit frames, 16 bits data
    - Total number of cards to build
  - Data rates
    - Assume 100kHz Level 1 accepts
    - Occupancy estimated to be 15% at $L=10^{34}$
    - Determines buffer sizes
  - Level 1 trigger crossing determination
    - Under study (Eno, Kunori, *etal*.)
    - Determines FPGA complexity and size (gates and I/O)

Region	Towers	Fibers	Trigger Towers
Barrel	4,968	2,304	2,304
Outer	2,280	1,140	0
Endcap	3,672	1,836	1,728
Forward	2,412	1,206	216
Total	**13,332**	**6,486**	**4,248**

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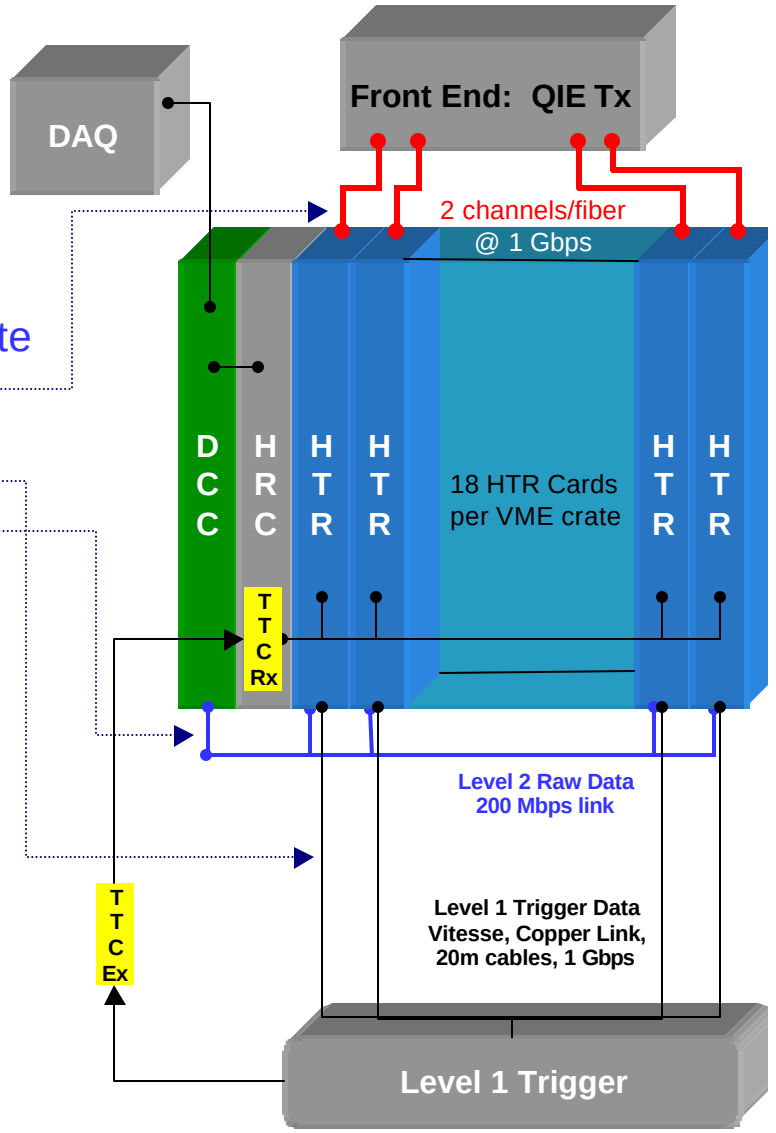
Readout Crate Components

- HCAL Readout Crate
  - 9U VIPA
    - No P3 backplanes and aux cards (saves $)
  - Receiver and pipeline cards:
    - 18 **H**CAL **T**rigger and **R**eadout (HTR) Cards per crate
      - Raw data fiber input
        - » 16 fibers, 2 channels per fiber=32 channels per card
      - Level 1 Trigger Primitives output
      - Level 2 Data output to DCC (next bullet)
  - Data Concentrator:
    - 1 DCC card (**D**ata **C**oncentrator **C**ard)
      - Receives and buffers L1 accepts for output to L2/DAQ
  - Crate controller:
    - 1 HRC card (**H**CAL **R**eadout **C**ontrol Module)
      - VME
      - CPU for slow monitoring
      - FPGA logic for fast monitoring
      - TTC LVDS fanout ala ECAL



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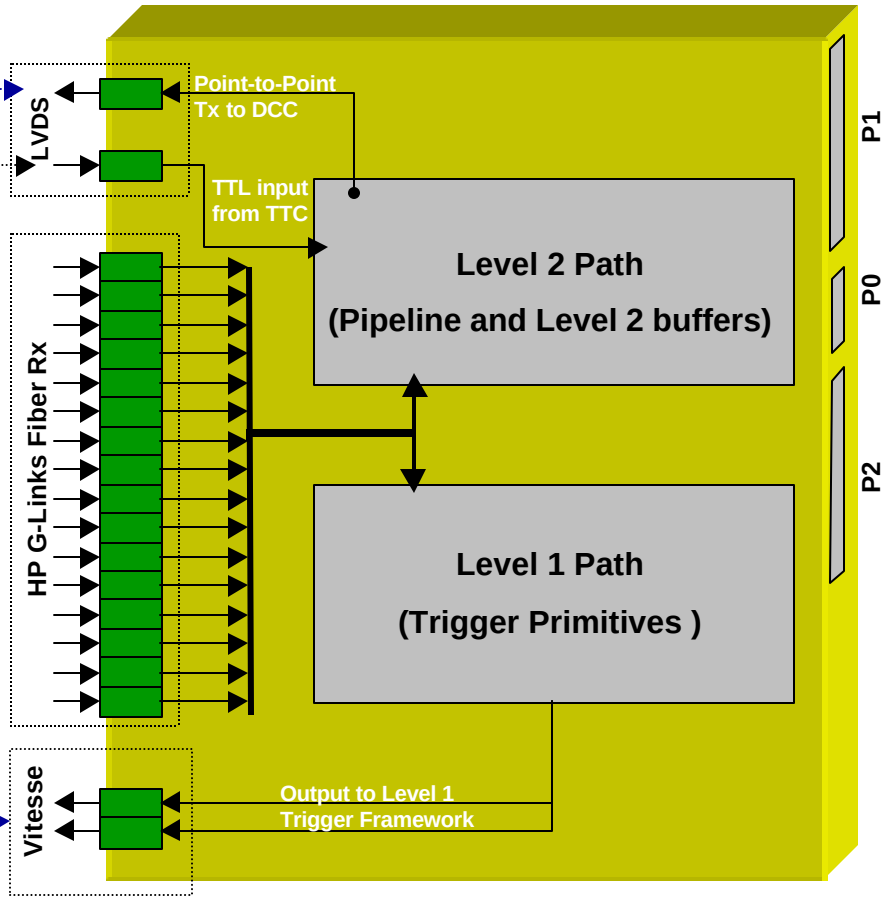
HCAL TRIGGER and READOUT Card

- All I/O on front panel
  - Level 1 Trigger Tower data outputs:
    - 8 shielded twisted pair
    - 4 per single 9-pin D connector
  - TTC input:
    - From TTCrx on HDC, ala ECAL
  - Raw data Inputs:
    - 16 digital serial fibers from QIE
    - 1 serial twisted pair with TTC information
  - DAQ data output to DCC:
    - Single connector running LVDS
- FPGA logic implements:
  - Level 1 Path:
    - Trigger primitive preparation
    - Transmission to Level 1
  - Level 2/DAQ Path:
    - Buffering for Level 1 Decision
    - No filtering or crossing determination necessary
    - Transmission to DCC for Level 2/DAQ readout



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HTR Card Conceptual Design

- Current R&D design focusing on
  - Understanding HCAL requirements
    - Interface with FNAL group
  - No card-to-card communication
    - Has implications with respect to summing in 53° region, and fiber routing
  - How to implement I/O
    - R&D on all relevant links is in progress
  - Minimizing internal data movement
  - FPGA algorithm implementation
    - Requires firm understanding of requirements
    - Requires professional-level FPGA coding
  - Reducing costs
    - FPGA implementation
      - Altera vs. Xilinx
      - On-chip FPGA memory is a big factor
    - Eliminating P3 backplane saves ~$1000/card and $1500/crate
    - Maintain openness to industry advances
      - “Watch” HDTV

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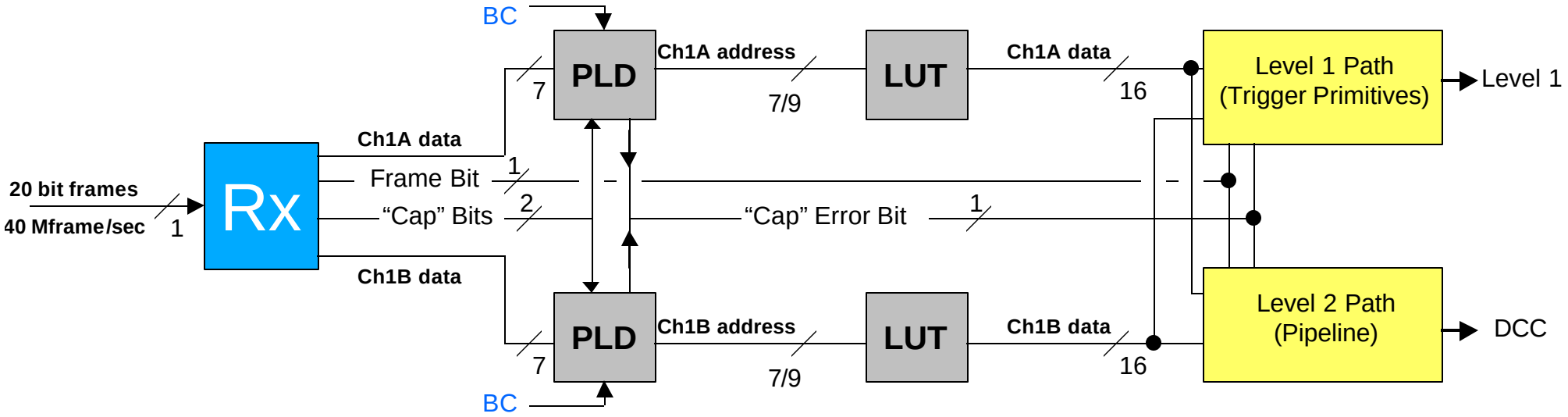
HTR Conceptual Schematic

- Input:
  - QIE 7 bit floating plus 2 bits “cap”
- Lookup table (LUT)
  - Convert to 16 bit linear energy
- Pipeline (“Level 1 Path”)
  - Transmit to Level 1 trigger, buffer for Level 1 Accept, 3 μs latency
- Level 2 Buffer (“Level 2 Path”)
  - Asynchronous buffer, sized based on physics requirements



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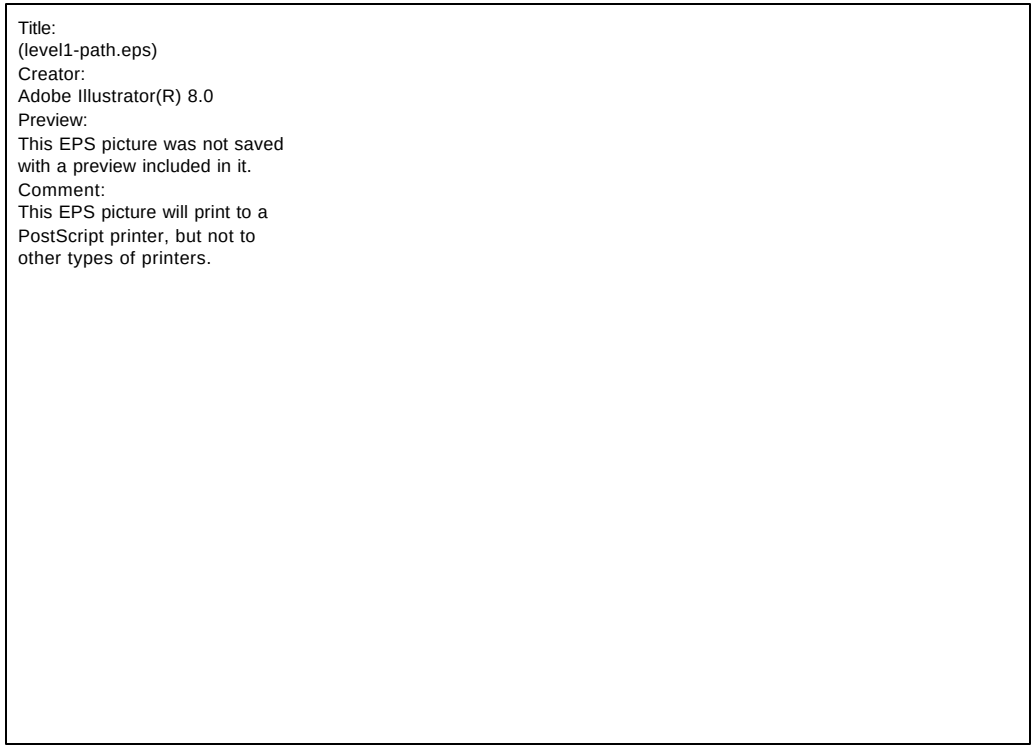
Level 1 Path

- 40 MHz pipeline maintained
- Trigger Primitives
  - 8 bit “floating point” E to 16 bit linear E_T
  - Combination of HCAL towers into TRIGGER Towers
  - Muon MIP window applied, feature bit presented to Level 1
- Relevant TTC signals via TTCRx chip
  - Synchronization and bunch crossing ID
- Level 1 Filtering using simple algorithm and BCID and Monte Carlo guides



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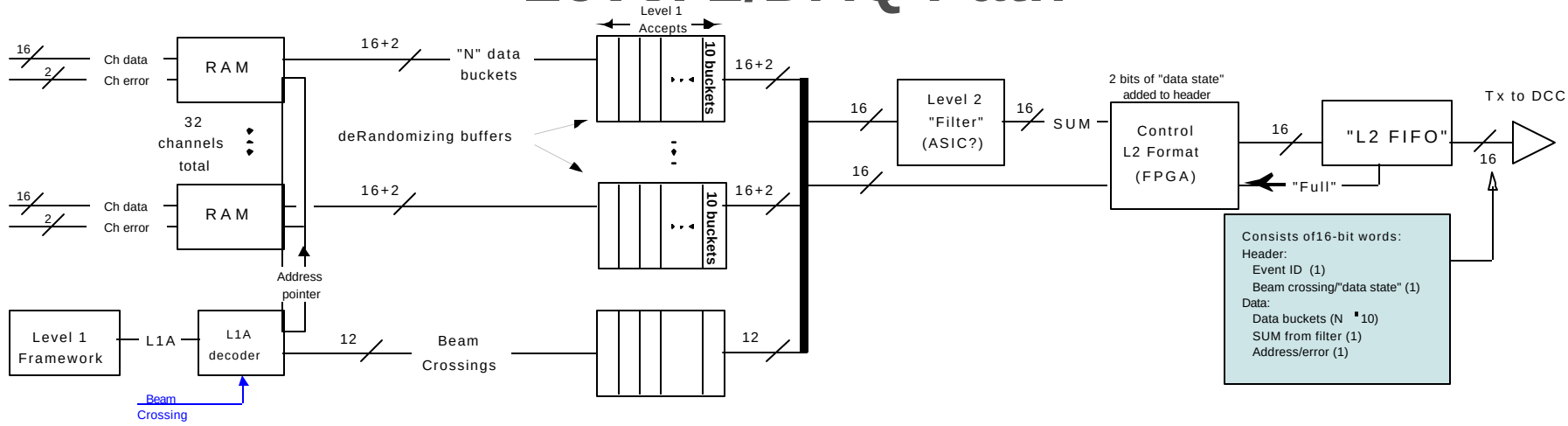
Level 2/DAQ Path



- 40 MHz pipeline into RAM, wait for L1 decision
  - 18 bits wide X 5μsec buffer = 3.6k bits/channel
  - 32 channels per card, 400kbits (see next slide)
- Level 1 Accept causes time slices clocked into derandomizing buffers
  - Assume 10 time buckets per crossing is necessary for readout
  - Apply HCAL proposed trigger rule: no more than 22 L1A per orbit
    - Deadtime < 0.1% given 100 kHz L1A
    - see “next” slide for more on this...

HTR Cost and Function Analysis

- HTR constitutes 60% of production M&S
- Cost estimates are difficult and very fluid due to uncertainty in requirements.
  - Driven by memory requirement:
    - 32 channels, 7 bits of raw data + 2 bits cap = 9 bits per channel
    - LUT produces 16 bits nonlinear, therefore needs 2^9=512 locations x 16 bits = 8192 bits per channel
    - Pipeline:
      - 5 μs latency (3 μs officially) requires 200 cells at 40 MHz
      - Store raw 9bits in pipeline, reduces memory requirement: 200x9=1800 bits per channel
    - Accept buffer (aka “derandomizer”)
      - How deep? Apply L1 Accept rule: < 15 L1A’s per orbit
      - 10 time buckets x 16 bits x 15 deep = 2.4k bits
    - Total bits/channel: 8192 + 1800 + 2400 = 12392
    - 32 channels means we need 400k bits
      - And that means we use the LUT in both L1 and L2 paths (ok, only 40 MHz pipeline, easy for FPGA)
  - There are some “tricks” but all have engineering risk and cost, *e.g.*
    - Do some integer arithmetic inside FPGA, save 2 cap bits, decrease memory by x4
    - Go off FPGA chip for memory access

HCAL L1A Limit Rule

- L1A average rate = 100 kHz = 1/10μs
  - 25 ns per crossing, means on average 400 crossings between L1A's
- Orbit period = 88 μs or approximately 3600 crossings
  - Therefore on average, 9.46 ± 0.36 L1A per orbit
  - We will require < 15 L1A per orbit for HTR L2/DAQ buffers

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HTR Costs

- FPGA:
  - Need 400k bits onboard memory
  - Need 32 channels x 9 pins input = 282 pins input
  - Need some VME + LVDS + Vitesse => another 100 pins at least
- Overall FPGA requirement: 400 kb memory, 500 I/O pins
- Latest quotes (as of 4/6/00, after baseline was established):

Vendor Part	*Gates (x1000)*	*Block Ram (kbits)*	*I/O Pins*		*Cost*
Xilinx 600E	986	295	316 444	BG432 FG676	$380 - $460
Xilinx 405EM	570	560	404	BG560	$267 - $450
Xilinx 1000E	1569	393	404 512	BG560 FG680	$750 - $1065
Altera 20K400E	1052	213	502	FG672	$335 - $475

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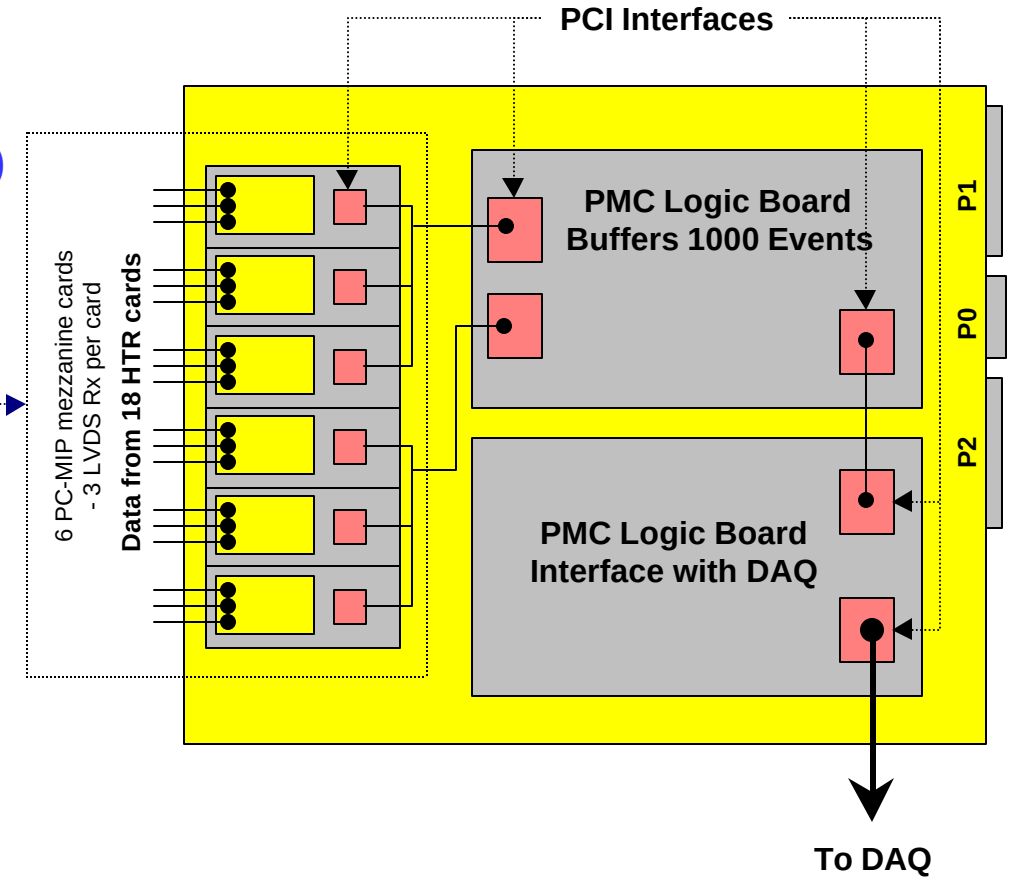
Data Concentrator Card

Motherboard/daughterboard design:

- Build motherboard to accommodate
  - PCI interfaces (to PMC and PC-MIP)
  - VME interface
- PC-MIP cards for data input
  - 3 LVDS inputs per card
  - 6 cards per DCC (= 18 inputs)
  - Engineering R&D courtesy of DÆ
- 2 PMC cards for
  - Buffering:
  - Transmission to L2/DAQ via Link Tx



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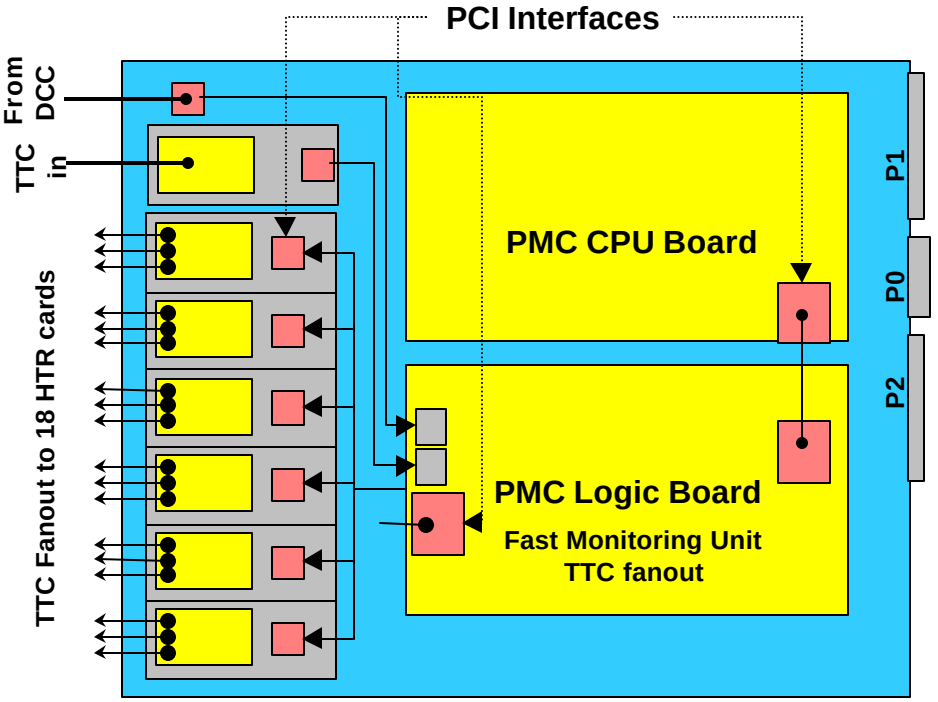
Hcal Readout Control Module

Motherboard/daughterboard design:

- Functionality:
  - Slower Monitoring and crate communication
    - PMC CPU, buy from industry
  - Input from DCC
    - To be determined
    - Monitoring and VME data path
  - TTC ala ECAL/ROSE
    - LVDS Fanout to all 18 HTR cards
  - Monitoring: (FMU)
    - FPGA implemented on PMC daughter board
  - Busy signal output (not shown)
    - To go to HCAL DAQ Concentrator (HDC)



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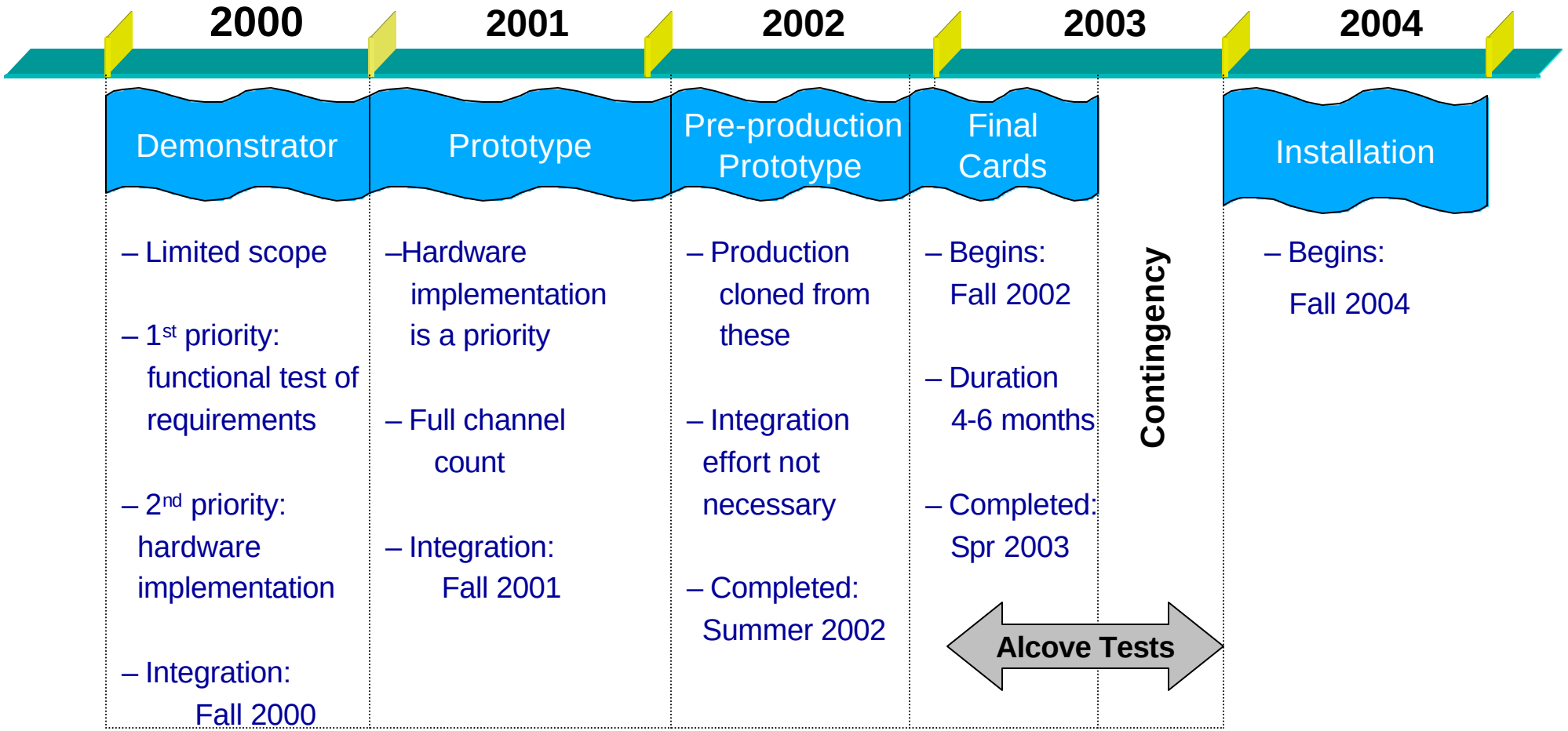
Overall Project Timeline



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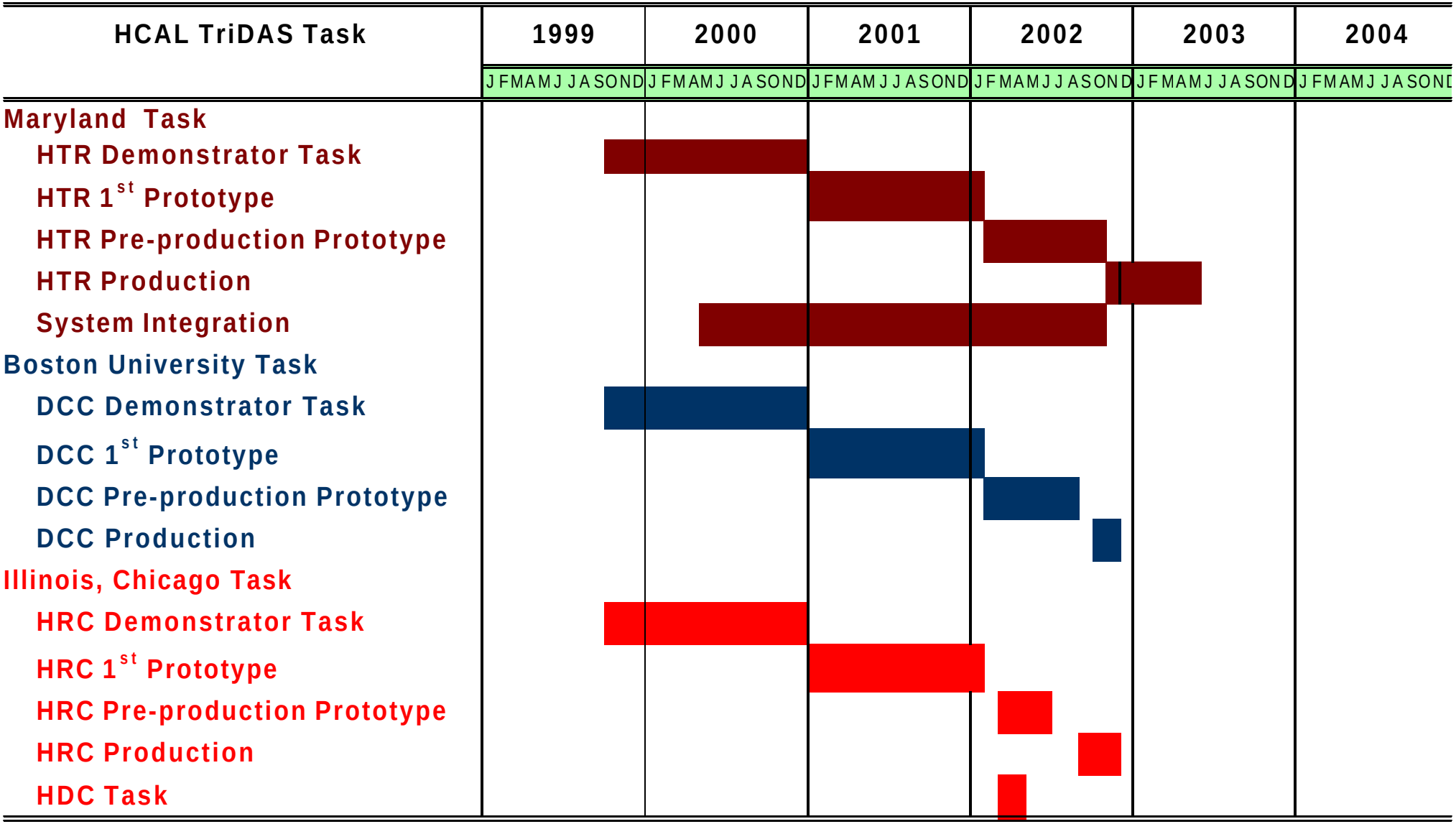
(Appendix)



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Project Status

- HTR project progress:
  - R&D on I/O proceeding: LVDS, Copper Gbit/sec (Vitesse), Fiber Gbit/sec (HP)
    - I/O board and HP G-link 6U front end emulator boards almost done
  - Evaluation of FPGA choices (no ASIC ala “Fermi”)
  - Better understanding of buffer sizes, synchronization, etc.
- DCC
  - R&D on DCC motherboard underway at BU
  - PC-MIP R&D underway, paid for from DÆ project
- HRC
  - UIC ramping up to provide some functionality of HRC card by fall 2000
- Integration
  - Synchronization issues under study (we are being educated)
    - HCAL will closely follow ECAL unless absolutely necessary
    - Mr. daSilva is helping us a great deal!
  - Plans to use early production cards for Alcove tests in early 2003
- Ready for TRIDAS integration:
  - Ready by beginning of ‘03
  - Preliminary integration tests possible after 1st prototype, somewhere in ‘02 maybe

Current Issues

- Parts cost
  - HTR implementation in 4 FPGA in 463 cards = 1852 FPGAs
  - Trying to pin down Xilinx and Altera
- Still learning about functional requirements, *e.g.*
  - how to design with uncertain crossing determination algorithm in HTR
  - How DDC interfaces with DAQ
  - Synchronization
- FPGA programming
  - Need to do this at the behavioral level
  - This is our biggest engineering concern, and we are doing the following:
    - Gain expertise in-house:
      - Verilog courses for Baden, students, engineers, *etc.*
      - Request help from Altera and Xilinx with FPGA code design
    - Mining expertise within the Masters level EE students
    - Tullio Grassi just hired (former Alice pixel engineer)
    - Confident that we will be ok on this..