HCAL TPG and Readout

CMS HCAL Readout Status

CERN

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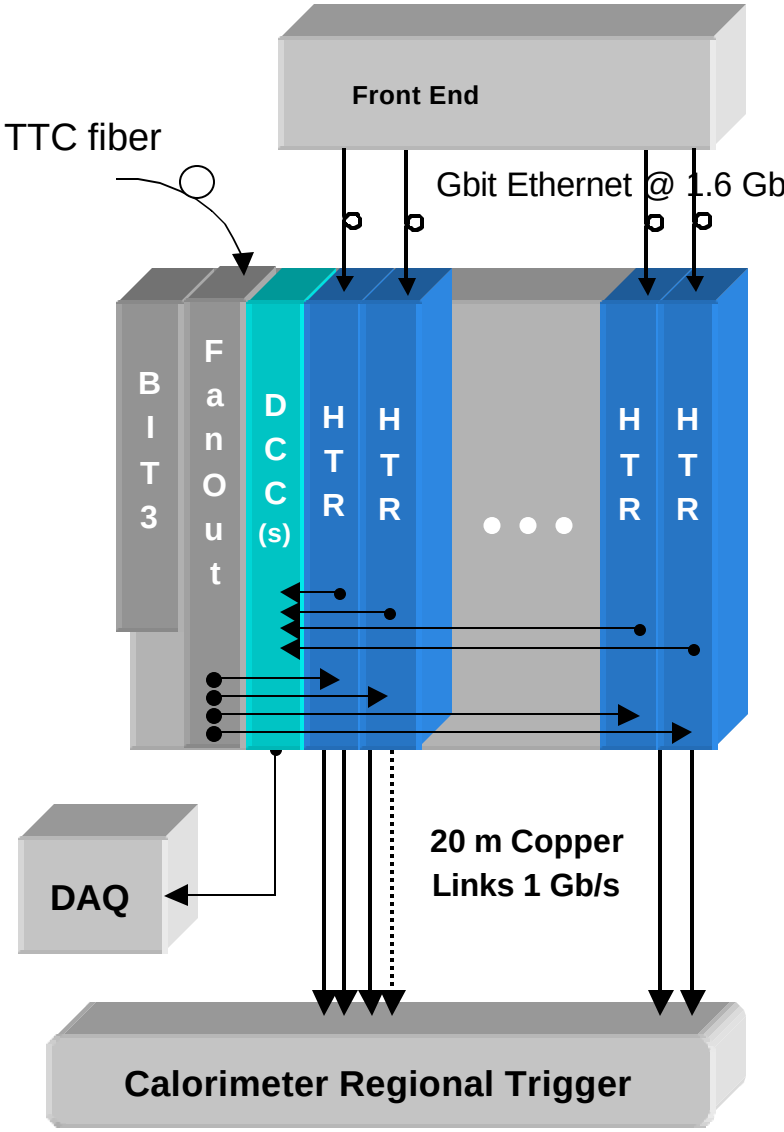
http://macdrew.physics.umd.edu/cms/

see also: *http://tgrassi.home.cern.ch/~tgrassi/hcal/*

Readout Crate Changes

- Outside world – slow monitoring, controls….
  - Bit3 PCI/VME interface
    - Known quantity
  - 3U Rack Computer
    - Dual processor DELL, fast PCI bus
  - Chris Tully to take responsibility
  - I'm keeping track of M&S for operations
    - Not yet added to WBS (I think….)
- UIC/HRC replaced by TTC/Clock Fanout
  - "HRC" did some of the above
  - Clock fanout is critical for VME crate functions
  - Fanout to all HTRs
- Fewer HTR/crate
  - Mapping considerations
  - Dual-width DCC considerations
    - Not yet settled. I don't like it…but we'll see…



HCAL TRIGGER and READOUT Card

No functional changes since Dec-2001

I/O on front panel:

- Inputs: Raw data:
  - 16 digital serial fibers from QIE, 3 HCAL channels per fiber = 48 HCAL channels
- Inputs: Timing (clock, orbit marker, etc.)
  - PECL
- Outputs: DAQ data output to DCC
  - Two connector running LVDS

TPG (Trigger Primitive Generator, HCAL Tower info to L1) via P2/P3

- Use aux card to hold Tx daughterboards
- Via shielded twisted pair/Vitesse

FPGA logic implements:

- Level 1 Path:
  - Trigger primitive preparation
  - Transmission to Level 1
- Level 2/DAQ Path:
  - Buffering for Level 1 Decision
  - No filtering or crossing determination necessary
  - Transmission to DCC for Level 2/DAQ readout

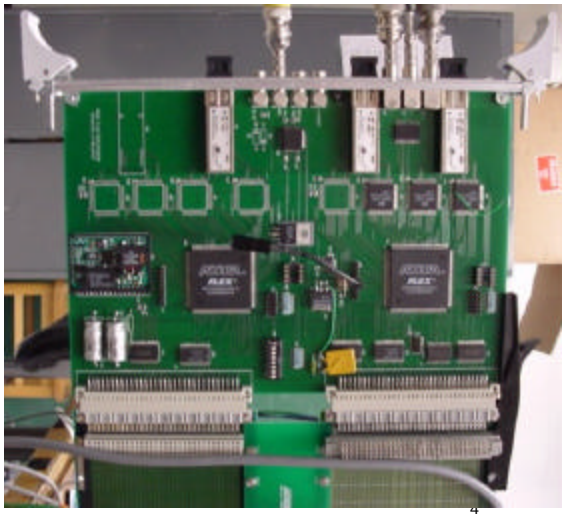
Demonstrator Status

Demonstrator

- 6U HTR, Front-end emulator
  - Data, LHC structure, CLOCK
  - 800 Mbps HP G-Links works like a champ
  - Dual LCs
- This system is working. FEE sends clock to HTR, bypasses TTC
  - HCAL FNAL source calibration studies in progress
  - Backup boards for '02 testbeam
    - Decision taken 3/02 on this (more…)
    - Anticipate we will abandon this card for testbeam
- DCC full 9U implementation
  - FEE ⇒ HTR ⇒ DCC ⇒ S-Link ⇒ CPU working
- Will NOT demonstrate HTR firmware functionality as planned
  - Move to 1.6 Gbps costs engineering time
  - Firmware under development now

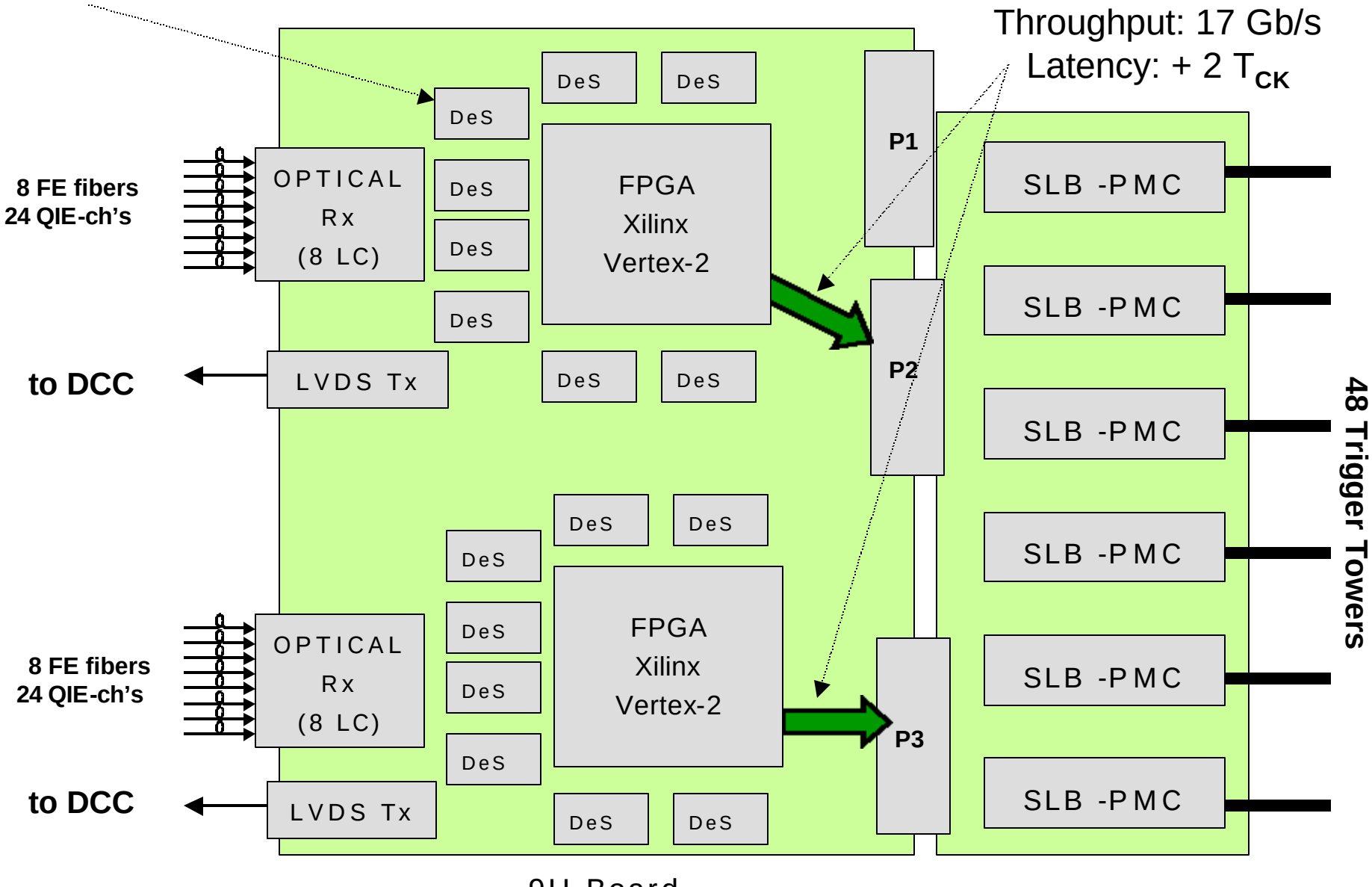
6U HTR

Demonstrator



6U FEE

HTR "Dense" Scheme



“Dense” HTR

- Dense (48 channel) scheme is now the baseline
  - Money
    - Fewer boards!
  - Programmable logic vs. hardware
    - Avoid hardware MUXs
    - Maintain synchronicity
  - Single FPGA per 8 channels
    - Both L1/TPG and L1A/DCC processing
  - Next generation FPGAs will have deserializers built in
    - Xilinx Vertex-2 PRO and Altera Stratix announced
    - Saves $500/board → $100k
    - ~20 connections to deserializer reduced to 1 connection at 1.6 GHz
    - Single clock would serve 8 deserializers
    - Probably won’t get to have any of these chips until summer 02….schedule may not permit
      - We will keep our eye on this
  - 48 channels x 18 HTR x LVDS Tx to DCC exceeds DCC input bandwidth
    - So, need 2 DCC/crate (but fewer crates)

Prototype Status

TPG transmission changed

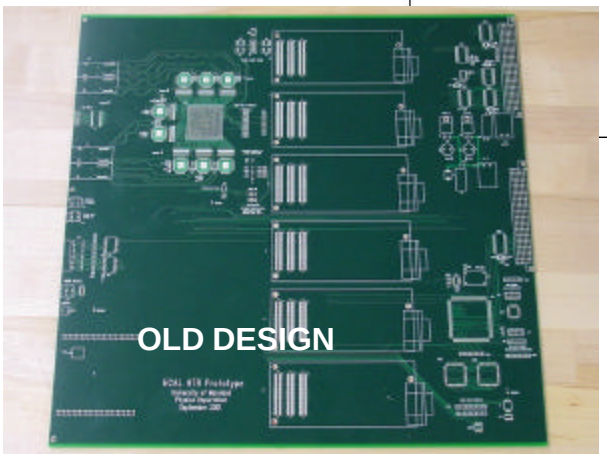
- From SLB mezzanine cards to Backplane aux card
  - Solves mechanical problems concerning the large cables to Wesley

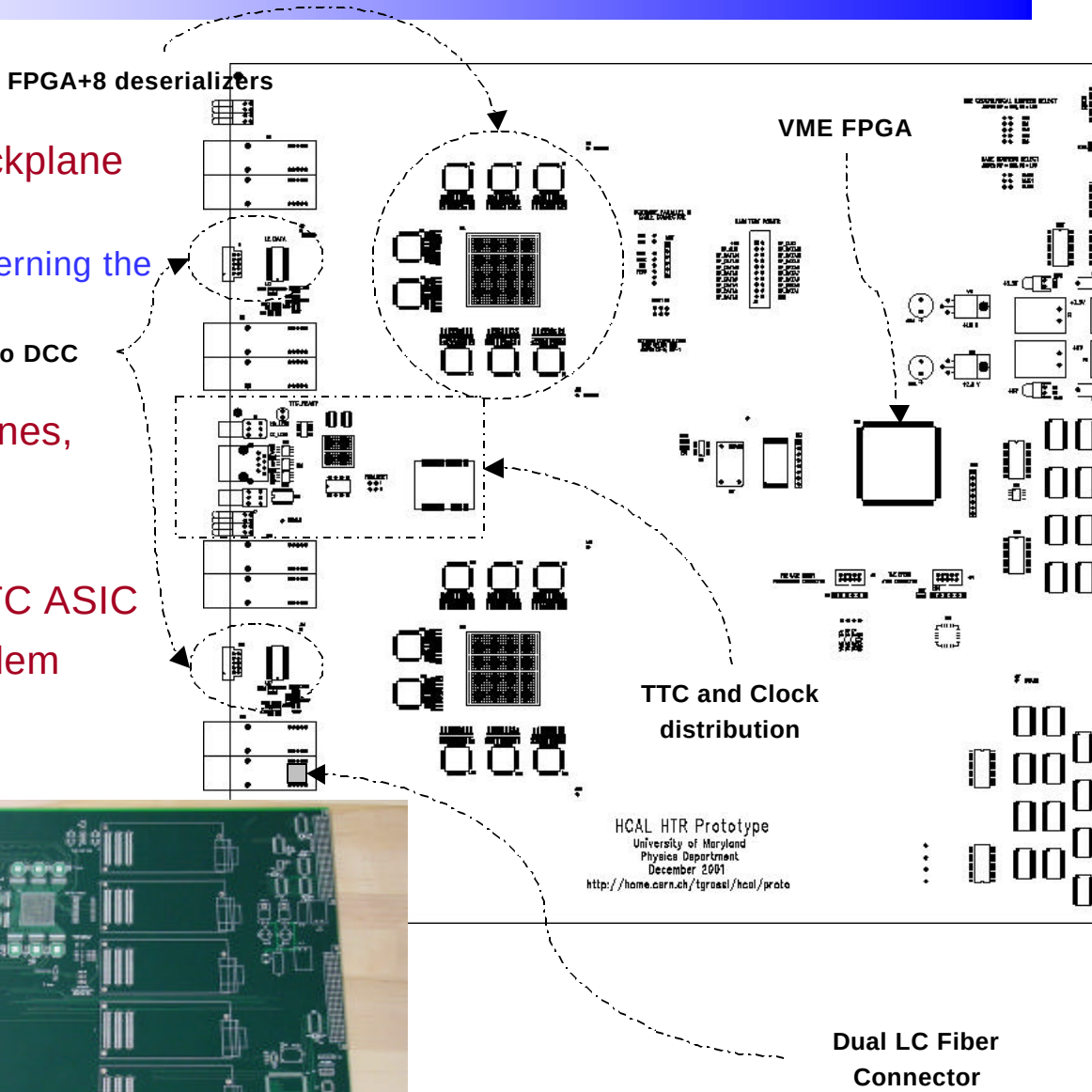
1.6 GHz link

- Wider traces, improved ground planes, power filtering, etc.
- Deserializer RefClock fanout
- TTC daughterboard changed to TTC ASIC
- Fixed TI deserializer footprint problem
- Clocking fixes

Next iteration estimate

- Submit in 2 weeks
- Stuffed and returned
- by April 1

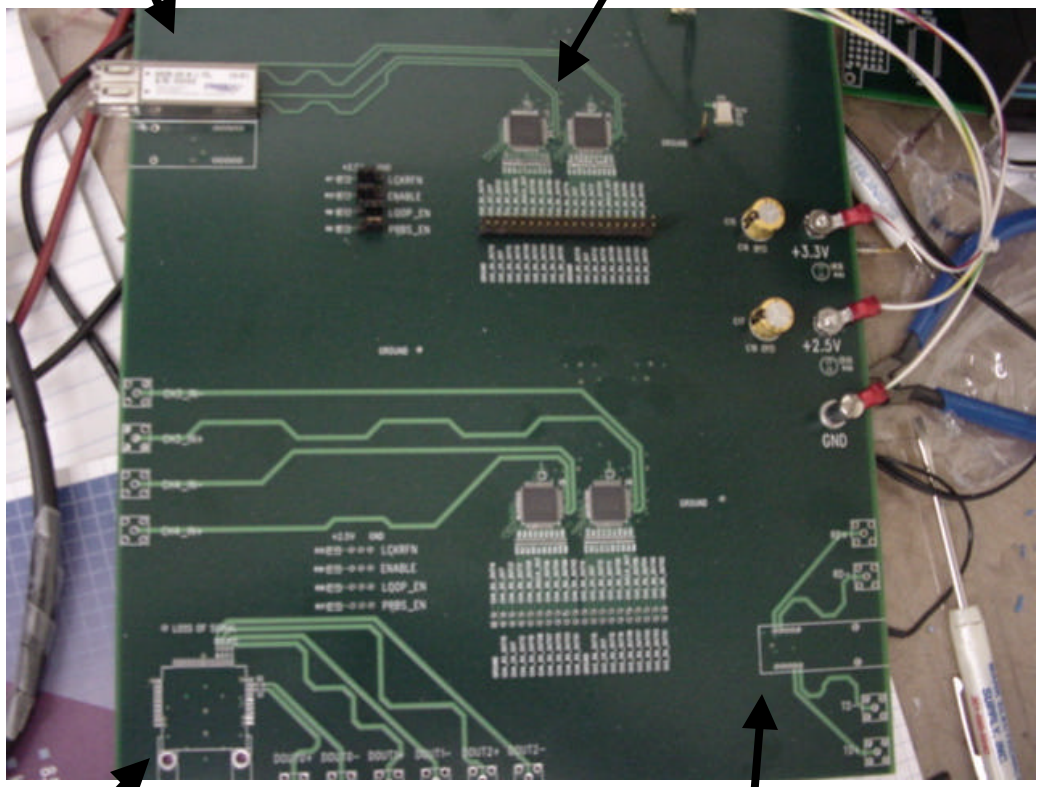




Current Hardware Status HTR

1.6 GHz link is the hardest part

- Made a “LinkOnly” board
- 2 dual LCs feeding 4 TI deserializers
  - TI TLK2501 *TRANSCEIVER*
  - 8B/10B decoding
  - 2.5Volts
  - 80MHz frame clock
    - 20 bits/frame
- Internal use only
- This board works.
  - We “know” how to do the link now
- Did not test the tracker NGK option



HTR Issues

Optical link

- Stratus LC's work well, available, not very expensive, probably will get cheaper.
- "Tracker solution"? We think no…this option appears to be dead.
  - NGK/Optobahn not responsive
  - Time scales for HTR is this summer
    - Tracker group has kept us at arms length with respect to vendors
    - Anticipate much ado about getting quotes and signing orders – schedule risk is too great
  - Savings is approximately $50/channel ($150k overall)
    - Expect LC's to get cheaper…will the NGK?

Clocking

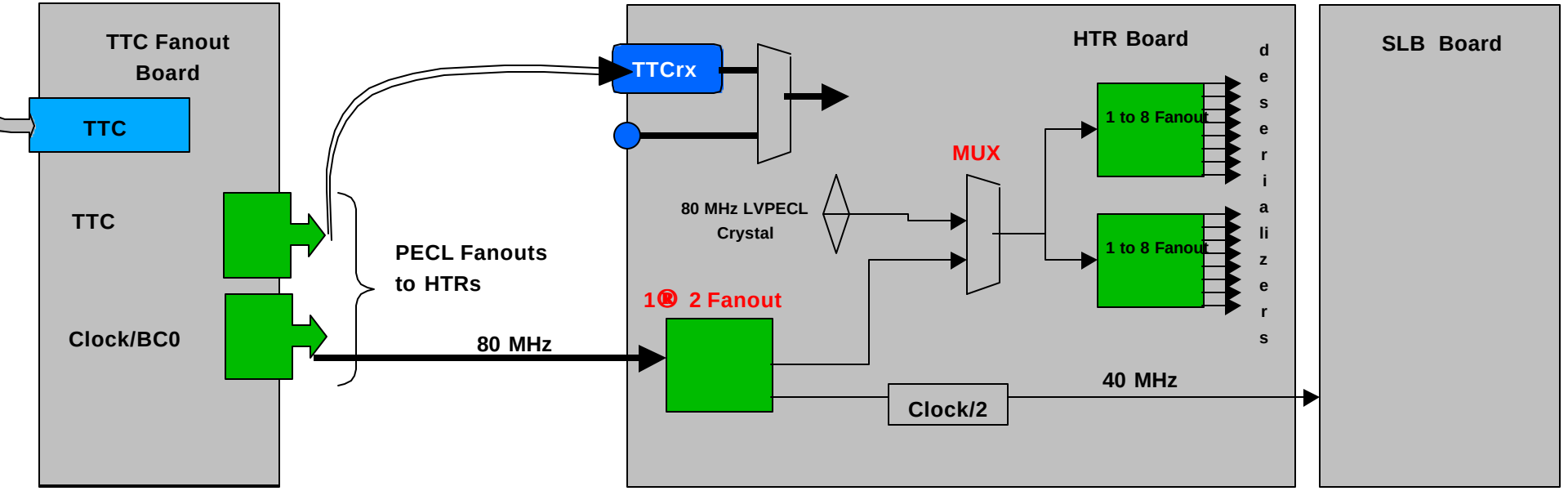
- Jitter requirements are surprising – refclk needs to be 80MHz ± ~30kHz to lock and stay locked.
  - This is because we are using a Transceiver, not a Receiver
    - TI does not have a Receiver – this is Gigabit ethernet, so it's meant for 2-way
  - We can implement in 2 ways
    - Onboard crystal
    - PECL clock fanout
  - Will have both for next iteration, board that will be in the testbeam summer '02

HTR Clocking

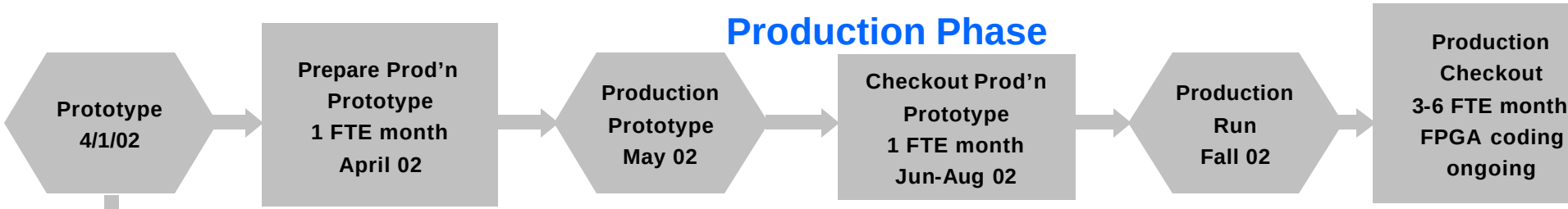
TTC provides input clock for the VME crate modules.

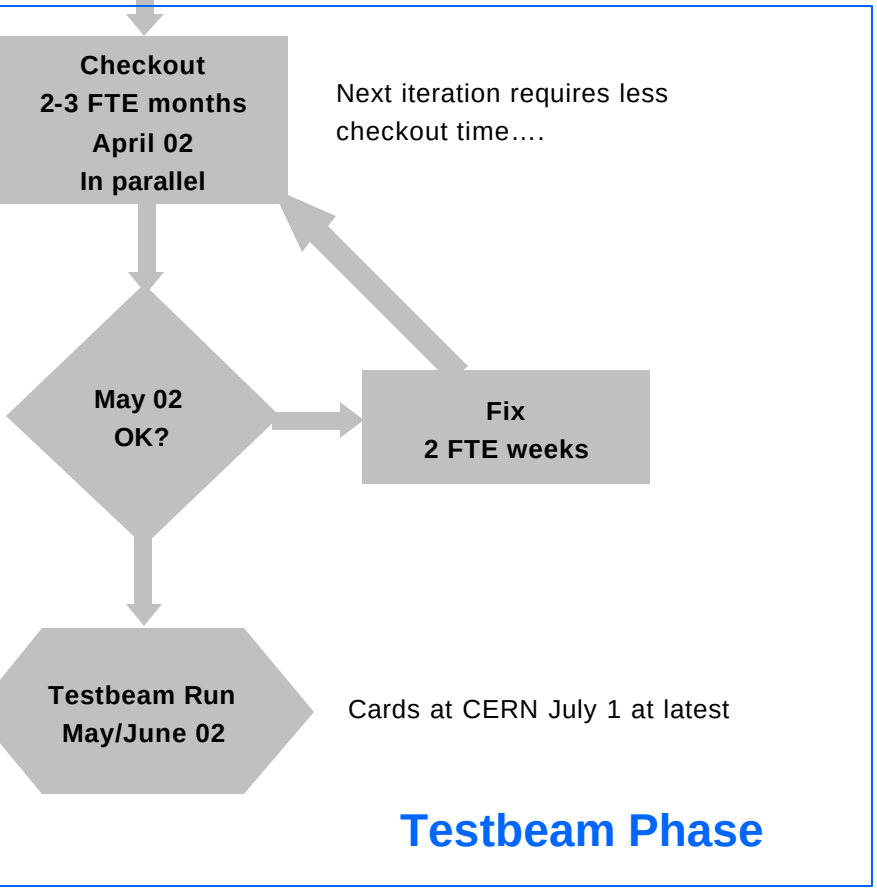
Clocks needed:

- DCC not critical
- HTR:
  - Deserializers (16) need 80MHz clock with ~40ps pkpk jitter
  - TPG transmission needs 40MHz clock with ~100ps pkpk jitter
  - Pipeline needs 40MHz clock synchronous with data transmission
  - Options – eliminate:
    - 80MHz crystal (eliminates 1 **Mux**)
    - TTC Fanout Board clock to deserializers (eliminates **1® 2 Fanout** and 1 **Mux**)
    - We will see what we learn at the Testbeam '02



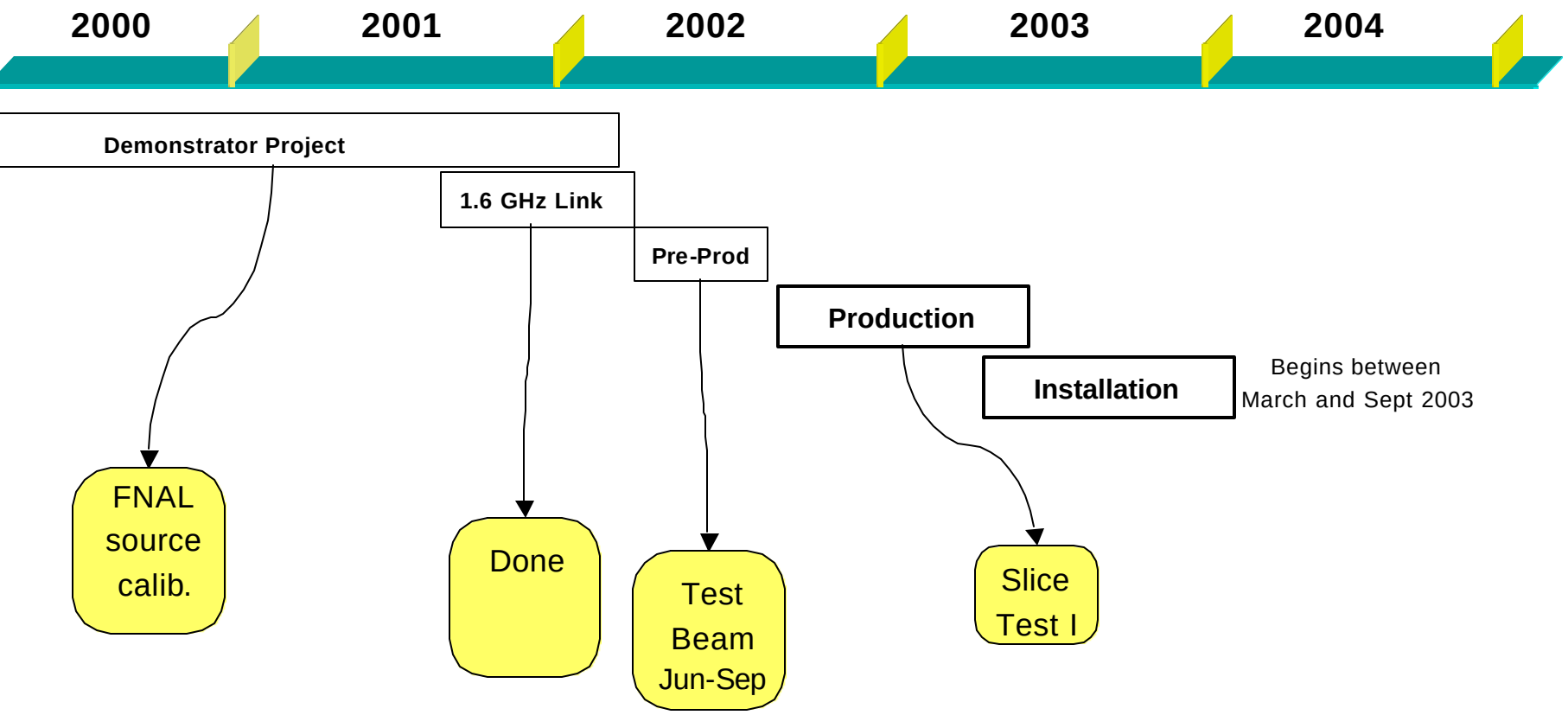
HTR Schedule





- Testbeam Phase
  - Next Checkout: 3 months
  - Fix problems: 0.5 months
  - Next checkout if needed: 1 month
- Production Phase
  - Prep for next pre-production run: 1 month
  - Checkout for production prototype: 1 month
  - Production checkout: 3-6 months
- FPGA coding: 6 months ?
- Total: 1.5 FTE years, around $180k
- Integration: ongoing…difficult to say

Current Project Timeline



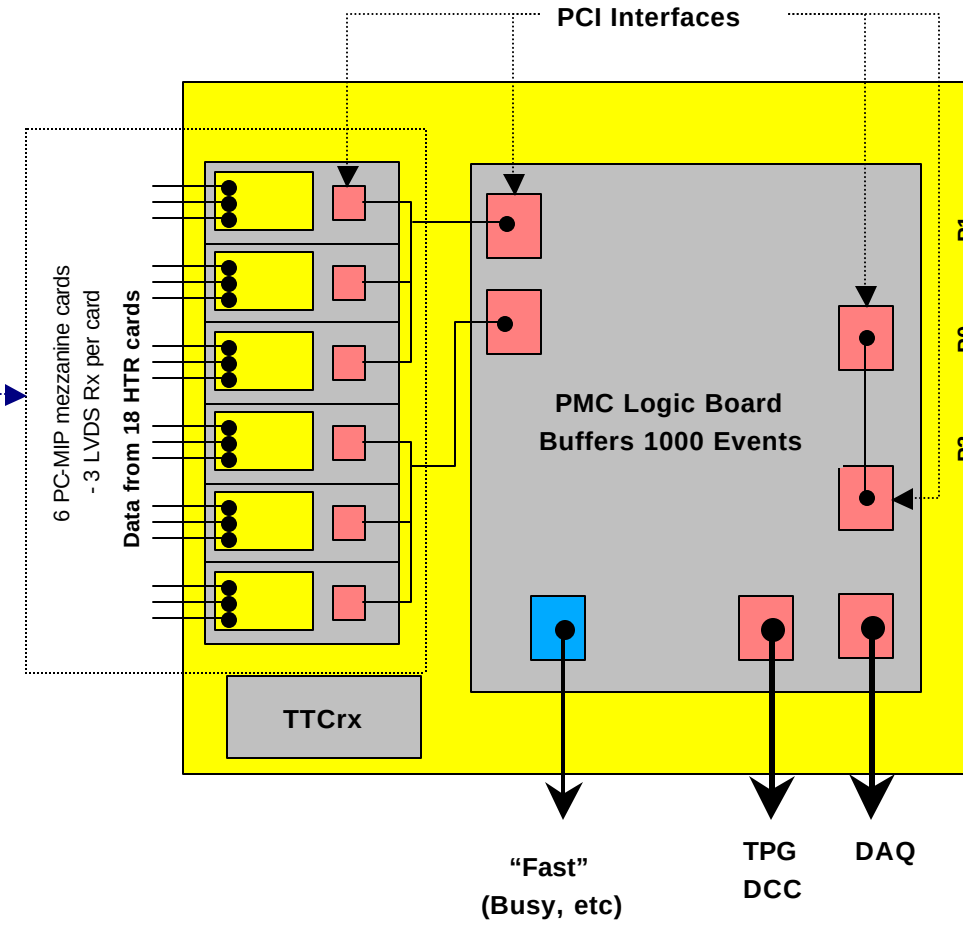
STILL SOME UNCERTAINTIES…

- Vertex-2 PRO or Altera Stratix
- Global clocking scheme
- Clock jitter

DATA CONCENTRATOR CARD

otherboard/daughterboard design:

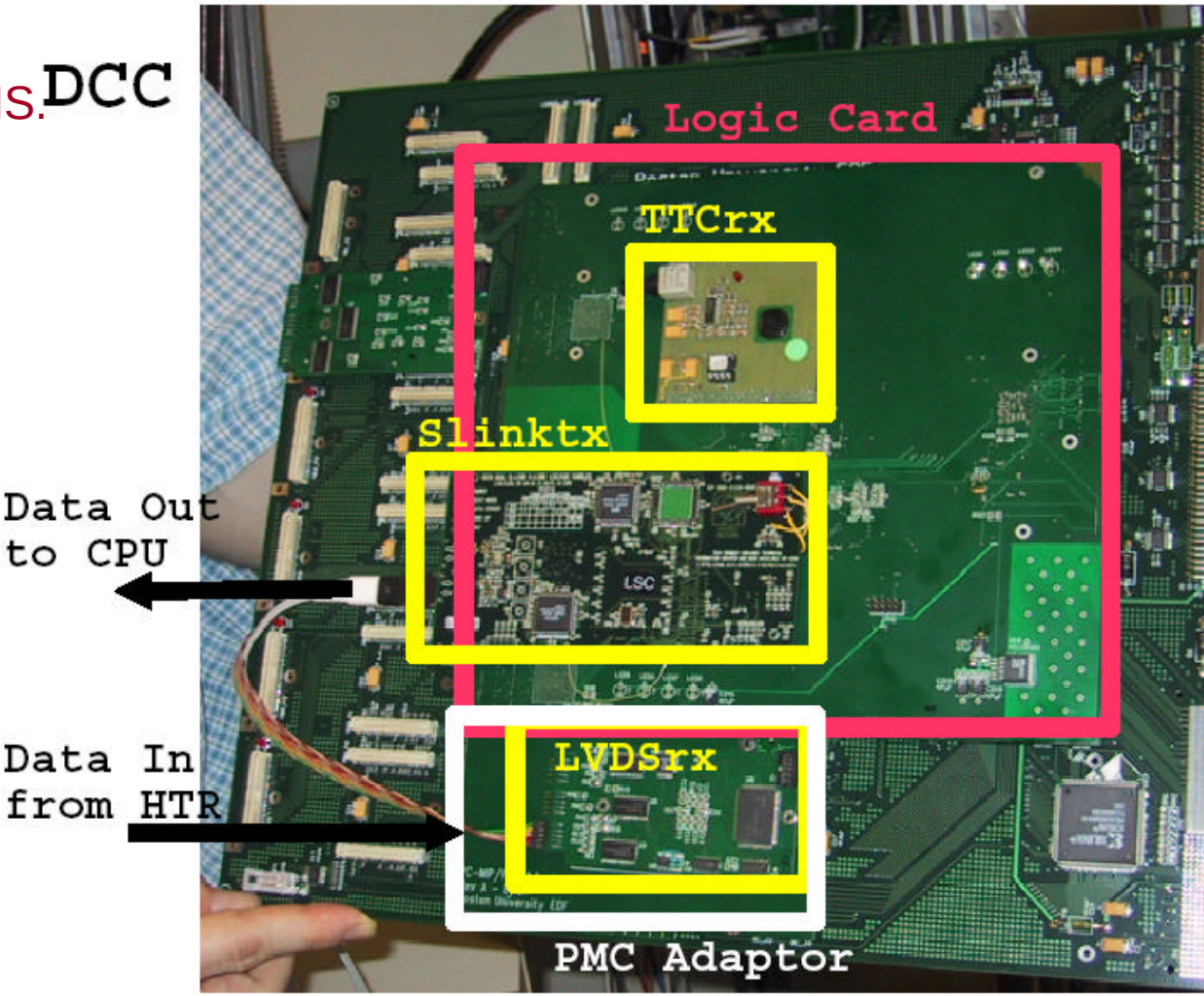
- VME motherboard to accommodate
  - PCI interfaces (to PMC and PC-MIP)
  - VME interface
  - *In production (all parts in house)*
- PC-MIP cards for data input
  - 3 LVDS inputs per card
  - 6 cards per DCC (= 18 inputs)
  - Engineering R&D courtesy of DÆ
  - *In production (purchasing underway)*
- Logic mezzanine card for
  - Event Building, Monitoring, Error-checking
  - S-Link64 output to TPG/DCC and DAQ
  - Fast busy, overflow to TTS
  - Giant Xilinx Vertex-2 1000 (XC2V1000)
- Transmission to L2/DAQ via S-Link



Current Status DCC Motherboard

VME Motherboard

- Production starting
- 5 prototypes in hand for CMS.
- All production parts bought
- PCB / Assembly order
  ~ May ‘02



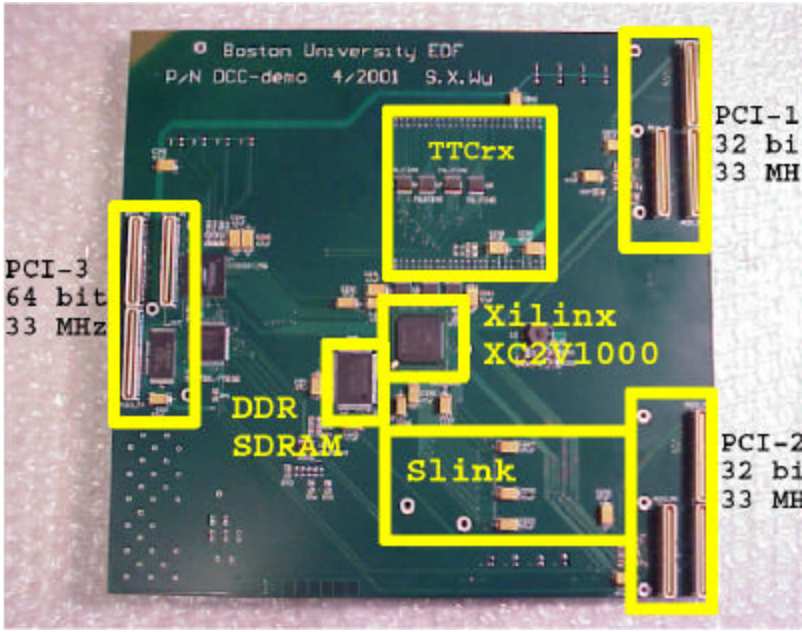
Current Status DCC Logic Board and LRBs

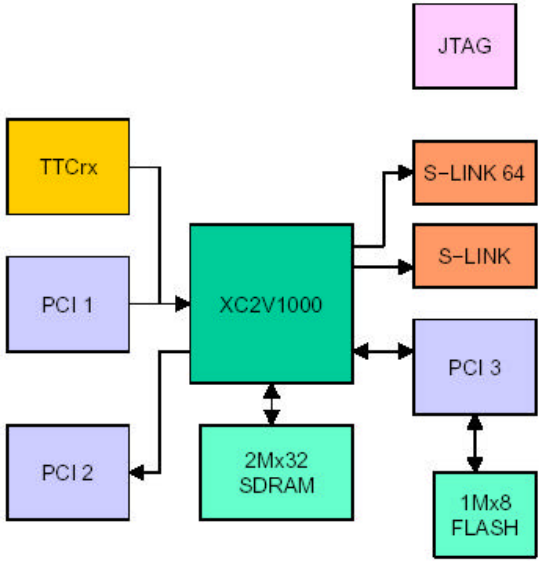
PC-MIP Link Receiver

- Design approved except for change to RJ-45 connector for links
- Final prototype PCBs on order
  Production parts on order
- Production to start ~ June '02

Logic Board – final prototype

- Decisions about S-Link
  Data Width / Card location
- Expect final PCB design late CY 2002
- Production in early 2003; driven by final decisions about functionality





HCAL TIMING FANOUT Module

- Fanout of TTC info:
  - Both TTC channels fanout to each HTR and DCC
  - Separate fanout of clock/BC0 for TPG synchronization
    - “daSilva” scheme
- Single width VME module

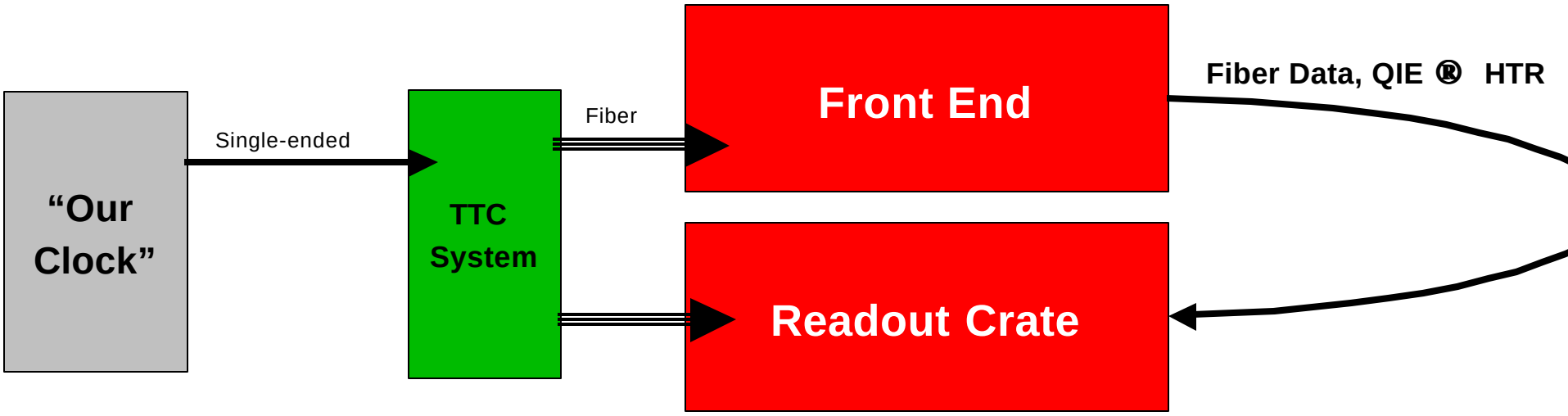
Testbeam Clocking

The only sane thing is to run the entire setup from a single high purity clock

- TTC input is single-ended LIMO.
- Source of “our clock” had better be clean.
- Chris will make us a 6U VME board
  - 35MHz crystal, care taken on transmitter. Will be in same VME crate as TTC
  - Can also put 30MHz, 37MHz, 40MHz…jump selected for playing around

We will have the same high quality clock for Tx and Rx

- HTR will have Crystals as a backup just in case….



Cost to Completion – M&S

Not much change in DCC, VME Rack, VME Crate unit costs

HTR cost increases by ~7%

- $320/board due to:
  - $100/board due to quality requirements on traces (need constant impedance lines)
  - $100/board for clock circuitry (Xtal, PECL stuff, etc.)
  - $120/board for LC's (old estimate was based on quads, but we're going with duals)
- Addition of HTR backplane card to support 48 channel HTR – net savings
- Cost decreases will surely come, but we don't know now.
  - LC's will only go down in price
  - TI deserializers are transceivers, receivers will be cheaper, TI will have to compete…FPGAs w/deserializers….

HRC replaced by TTC Fanout + Bit3 + Crate CPU

Mapping really constrains us

- Some HTR will not be full of SLBs
  - Still requires 1 SLB transition card per HTR
- Some crates will not be full of HTRs
  - Original cost had up to 18 HTR/crate, now it's around 14
- Results in a few more crates than 9/01 cost estimate

Cost to Completion – M&S (cont)

Item	9/01		3/02		
	Unit	Total ($k)	Unit	Total ($k)	Comment
	$4.8k	$1043	$5.1k	$1128	Includes LED cards plus 7% increase per card
Crates	$5.5k	$ 72	No change	$ 88	3 more crates from mapping considerations
Racks	$3k	$ 18	No change	$ 24	2 more racks, 2 crates/rack
	$5k	$ 150	No Change	$ 180	3 more crates, 2 DCC/crate
: SLB+TPG es+SLB_HEX	$100+$100+$0	$ 110	$100+$100+$300	$ 176	SLB transition boards, already added to 2.1.7.15
C"	$5k	$ 85			Old project, changed to…
C Fanout			$1.5k	$ 40	Current UIC project, based on best guess for Fanout
3 (VME+PCI s + fiber)			$3.8k/crate	$ 61	Not accounted for in HCAL TriDAS Lehman 2000
ck Computer			$2.9k/comp	$ 23	Not accounted for in HCAL TriDAS Lehman 2000
AL:		$1478	$1720		$242k difference: HTR additions: $85k SLB transition card: $66k added Bit3/Rack Computer: $84k never costed before? More Racks/Crates: $52k due to mapping TTC Fanout: $40k change of task Total Reductions: $85k HRC change of task

HTR Itemized Cost (Appendix)

- Costs as of April 2001….
  - 12 fibers/card, 3 channels/fiber

Lehman 01 slide

FPGA (4 per card)	$750	4x$750=$3k ® 2x$1.2k=$2.4k
PC Board (from D0 project)	$200	Tullio doesn't believe it. Up to $500
Fab & Assembly	$200	Tullio doesn't believe it. Up to $400
Fiber Receiver (PAROLI)	$480	$640 for 16 dual LC's
Deserializer receivers	$430	8 vs. $580 for 16
Vitesse/LVDS	$ 50	
Connectors (no P3!)	$200	
Misc (FIFOs, MUX, VME, etc)	$400	TTC/clock circuitry since then
Total	**$2,710**	X2 = $5420 v. $5120 without reductions

Additional M&S Costs

Test stands never accounted for

- $29k/crate total
- Proposal calls for 3 test stands - $87k total
  - 1 @ FNAL
  - 1 @ UMD/BU/Princeton
  - 1 @ CERN
    - This one used for testbeam and then moved to USCMS electronics area

1 VME crate	$5,500
1 VME Rack Computer	$2,900
1 Bit3 w/fiber	$3,820
2 HTR	$10,252
1 TTC fanout	$1,500
1 DCC	$5,000
Total	$28,972

"EM Trigger"

- Rohlf estimates 1 crate ($5.5k), 2DCCs ($10k), 12 HTR ($62k)
- If we need additional Bit3 and CPU, it's another $6.7k
- Total would be $84k

Testbeam

- We will be producing HTRs that may, or may not, be final versions.
- If so, no problem. If not, additional costs
- Estimate around 6 HTR including 2 spares, comes to around $40k

Cost to Complete – Effort BU/UIC

Difficult to predict

- UMD: 1.5 FTE years (previous slide)
- BU 1.5 FTE years
  - Testbeam extra work: 3 FTE months
  - Finish DCC prototype (FPGA code): 4 FTE months
  - DCC “final prototype”: 6 FTE months
    - SLINK64, 2-slot or Transition board…
  - Test engineering: 2 FTE months
- “UIC”
  - 1 FTE engineer, should be finished with TTC fanout by Fall 02
  - FNAL might want to keep him around to help with system clock issues

Project Status Summary

HTR (Maryland):

- 6U Demonstrator done
- Testbeam Effort
  - OK if no disasters
  - But…integration is going to be a big effort and will interfere with Production effort
- Production Effort
  - FPGA coding ongoing
  - Will work on HTR in parallel w/testbeam effort

TTC fanout

- First board assembled and tested
- Next iteration underway - Will be ok for testbeam

Crate CPU issues

- Chris Tully is playing with Bit3 and DELL 3U rack mounted dual CPU

DCC

- 9U Motherboard done., PCI meets 33MHz spec, Production run beginning
- Link Receiver Cards - Built, tested, done.
- Logic board
  - Underway. Only issues are FPGA Coding, Backplane card vs. double-width