HCAL TPG and Readout

CMS HCAL Readout Status
CERN

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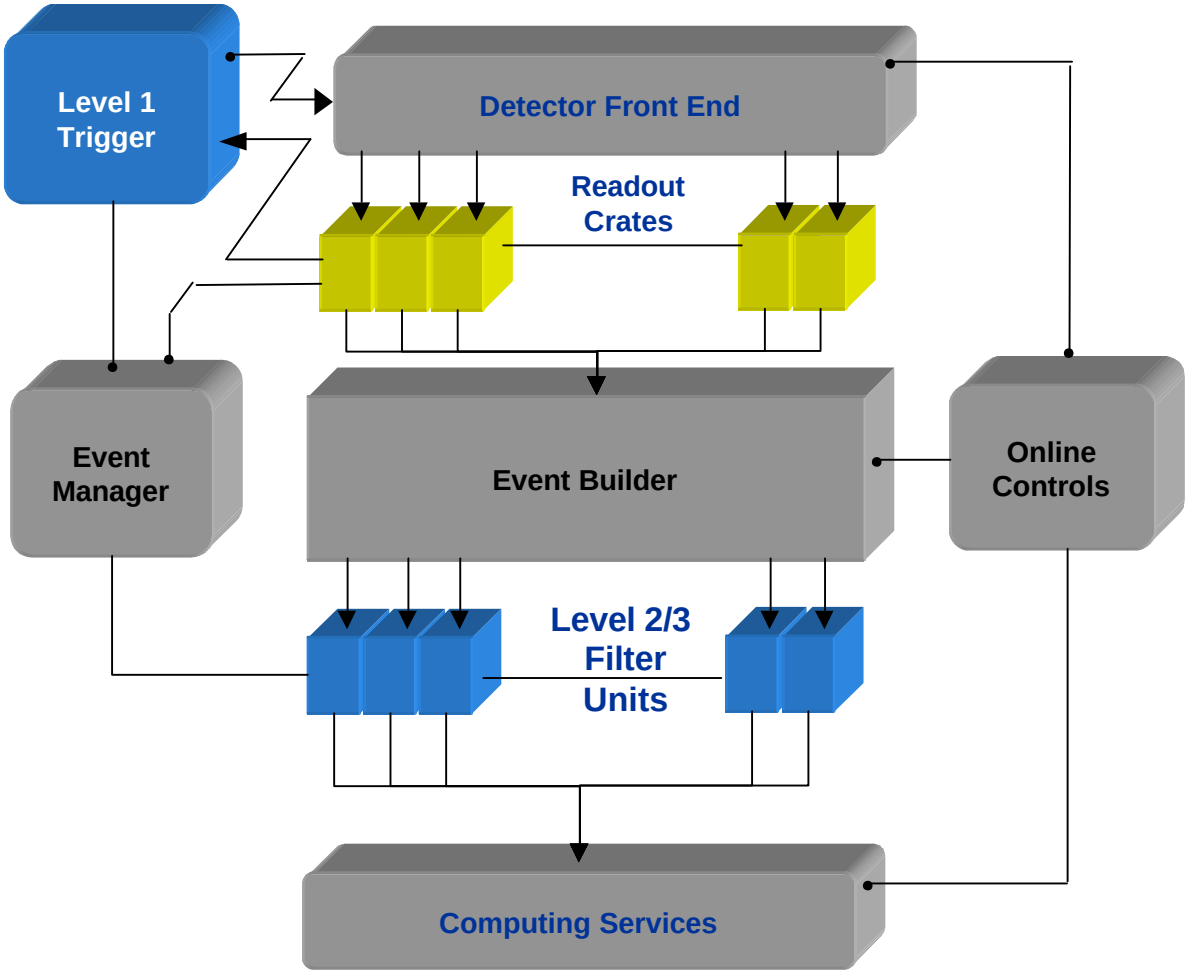
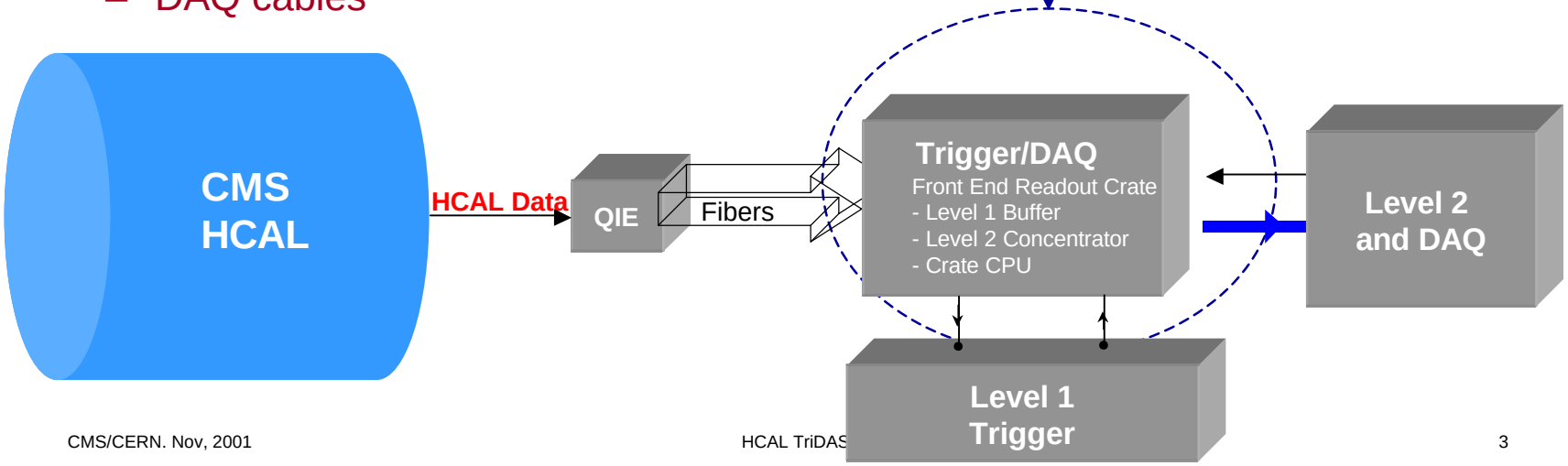
CMS TriDAS Architecture

- Data from CMS FE to T/DAQ Readout Crates
- Level 1 “primitives”
  - Crossing determined
  - Summing
  - Tx to Level 1 Trigger
  - Data is pipelined waiting decision
- Level 1 accepts cause
  - Tx raw data to concentrators
  - Buffered and wait for DAQ readout
- System communication via separate path (TTC)
  - Clock, resets, errors, L1 accepts…

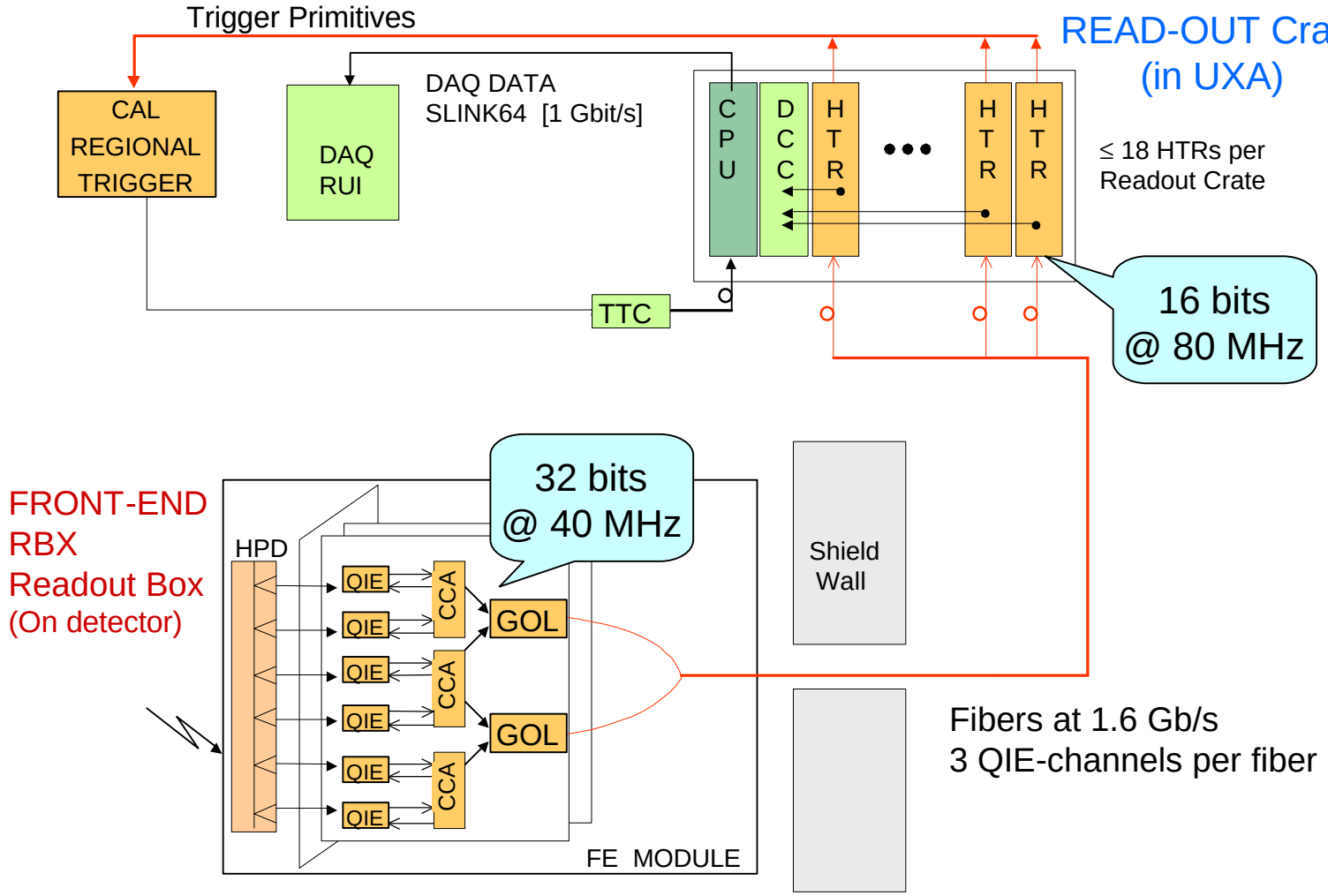


HCAL Contribution to T/DAQ

- Includes:
  - Receiver cards (including fiber input receivers and deserializers)
  - Cables to Level 1 Trigger system
  - Concentrators
  - VME crate CPU module
  - VME crates and racks
- Everything between but not including:
  - Fibers from QIE FEs
  - DAQ cables

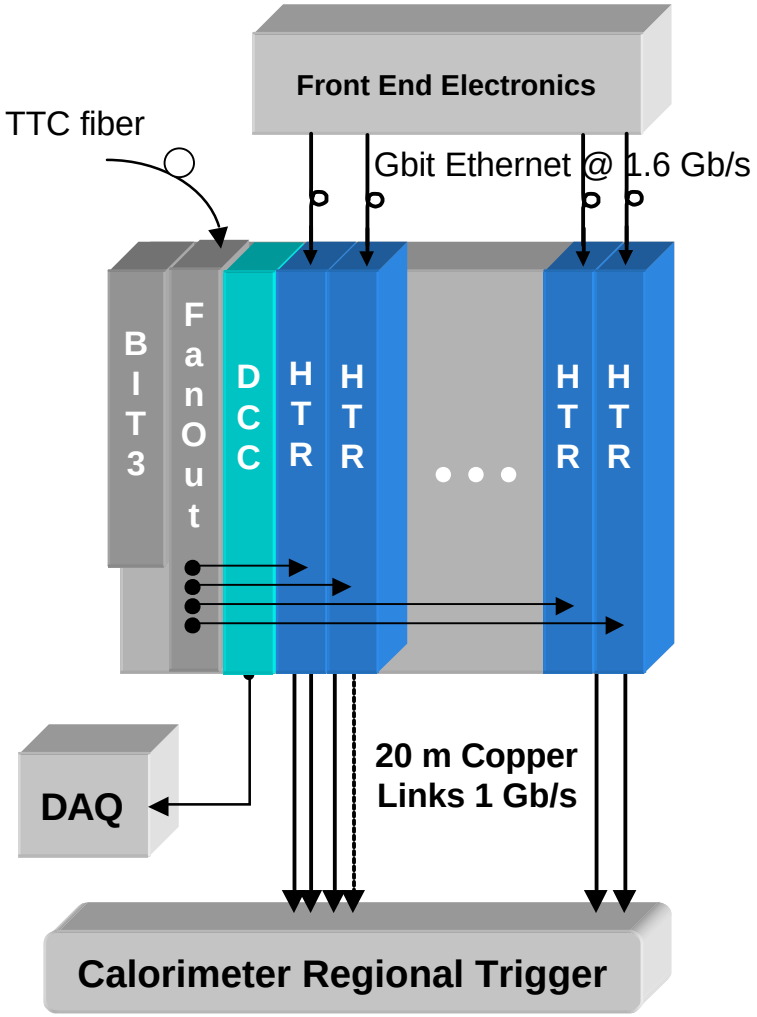


HCAL FE/DAQ Overview



Readout Crate Components

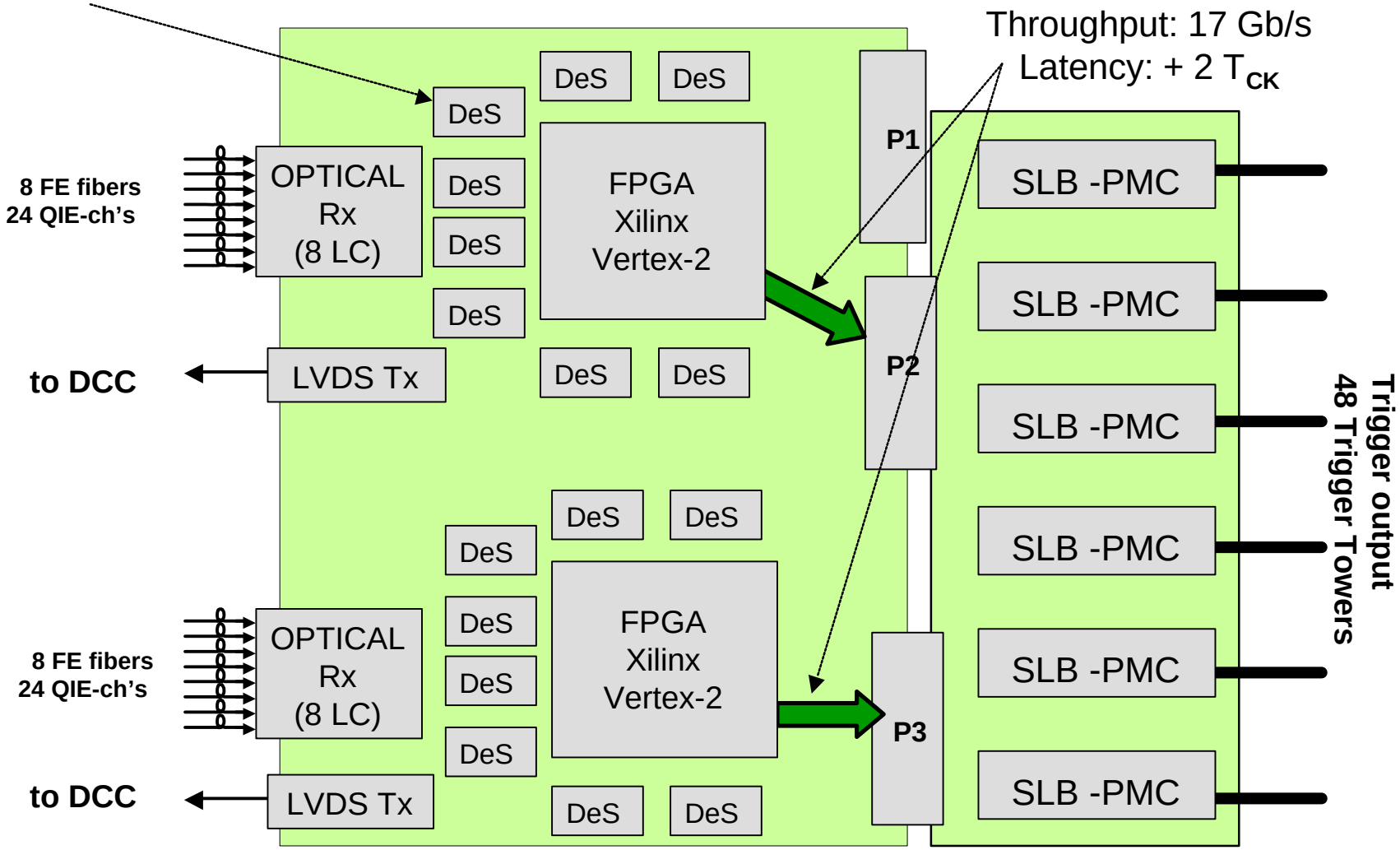
- **“BIT3”** board
  - Commercial VME/PCI Interface to CPU
  - Slow monitoring
- **FanOut** board
  - FanOut of TTC stream
  - FanOut of RX_CK & RX_BC0
- **HTR** (**H**CAL **T**rigger and **R**eadout) board
  - FE-Fiber input
  - TPs output (SLBs) to CRT
  - DAQ/TP Data output to DCC
  - Spy output
- **DCC** (**D**ata **C**oncentrator **C**ard) board
  - Input from HTRs
  - Output to DAQ
  - Spy output



HCAL TRIGGER and READOUT Card

- I/O on front panel:
  - Inputs: Raw data:
    - 16 digital serial fibers from QIE, 3 HCAL channels per fiber = 48 HCAL channels
  - Inputs: Timing (clock, orbit marker, etc.)
    - LVDS
  - Outputs: DAQ data output to DCC
    - Two connector running LVDS
- TPG (Trigger Primitive Generator, HCAL Tower info to L1) via P2/P3
  - Via shielded twisted pair/Vitesse
  - Use aux card to hold Tx daughterboards
- FPGA logic implements:
  - Level 1 Path:
    - Trigger primitive preparation
    - Transmission to Level 1
  - Level 2/DAQ Path:
    - Buffering for Level 1 Decision
    - No filtering or crossing determination necessary
    - Transmission to DCC for Level 2/DAQ readout

HTR – "Dense" scheme



“Dense” HTR

- Strong reasons to push to dense scheme
  - Money
    - Fewer boards!
  - Programmable logic vs. hardware
    - Avoid hardware MUXs
    - Maintain synchronicity
  - Single FPGA per 8 channels
    - Both L1/TPG and L1A/DCC processing
    - Xilinx Vertex-2 PRO will have deserializer chips built in!
      - Saves $500/board
      - Many fewer connections
      - ~20 DeS->FPGA connections replaced by 1 1.6 GHz line
      - Challenges:
        - » Layout of 1.6 GHz signals
        - » Schedule implications for final production may have to slip ~6 months to wait for Vertex-2 PRO
- What do we give up?
  - Each board much more epensive
  - More difficult layout
  - Need transition board to handle TPG output
    - So does ECAL – common solution will be used
  - Need 2 DCC/crate (but half the number of crates!)

Changes from HTR Demo to Final

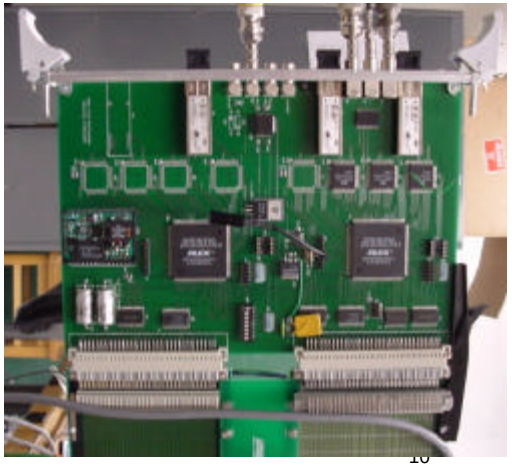
- Front-end input
  - From 800MHz HP G-Links to 1600MHz TI Gigabit ethernet
- Timing
  - TTC daughterboard to TTC ASIC
- Core logic
  - Altera to Xilinx
- Trigger output
  - Moved to transition board
- Form factor
  - 6U to 9U
- More understanding in general
  - Tower mapping, TPG sums, *etc.*

Demonstrator Status

- Demonstrator
  - 6U HTR, Front-end emulator
    - Data, LHC structure, CLOCK
    - 800 Mbps HP G-Links works like a champ
    - Dual LCs
  - This system is working. FEE sends clock to HTR, bypasses TTC
    - Will be used for HCAL FNAL source calibration studies
    - Backup boards for ’02 testbeam
      - Decision taken 3/02 on this (more…)
  - DCC full 9U implementation
    - FEE ⇒ HTR ⇒ DCC ⇒ S-Link ⇒ CPU working
  - Will NOT demonstrate HTR firmware functionality as planned
    - Move to 1.6 Gbps costs engineering time
    - Firmware under development now

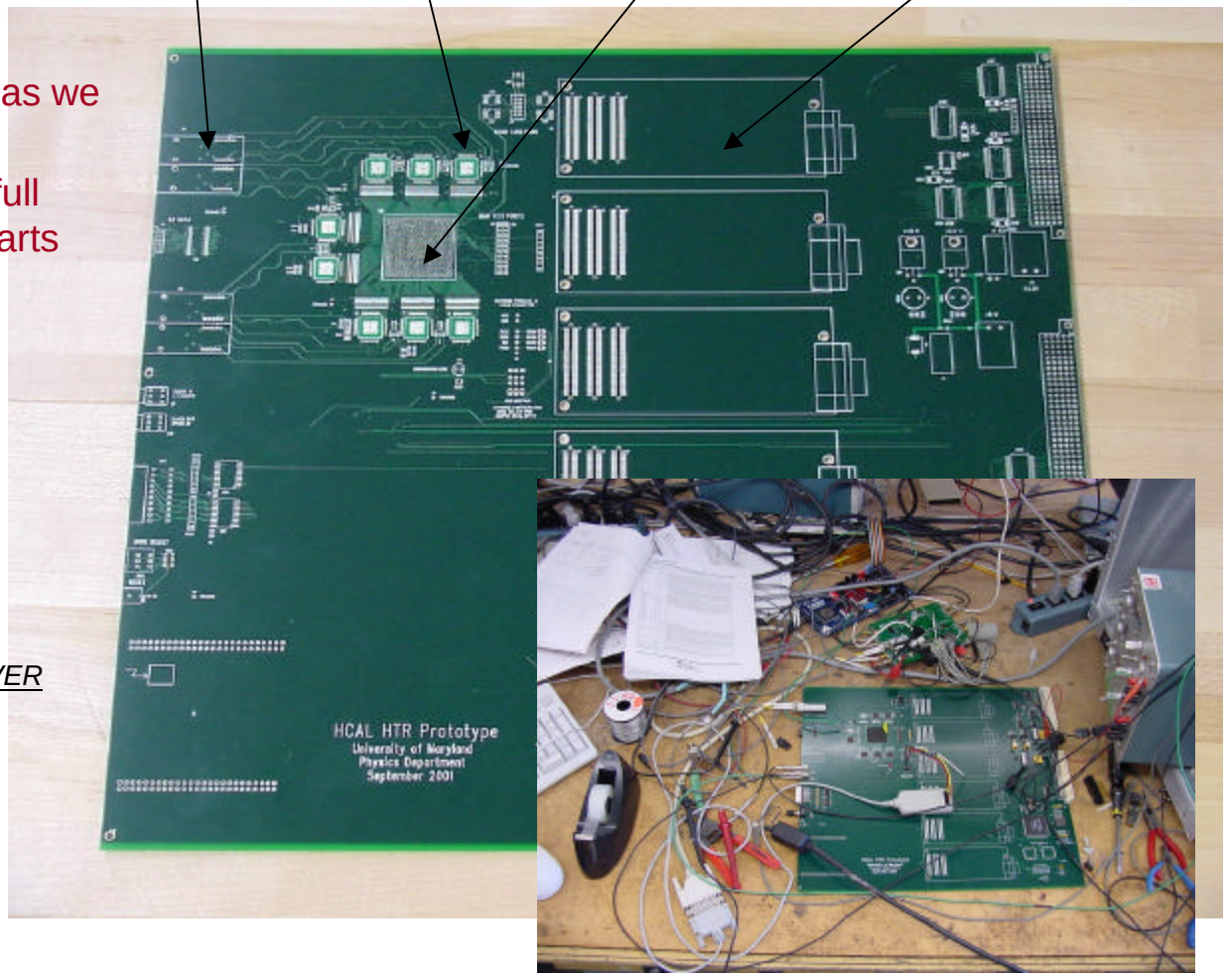
6U HTR Demonstrator

6U FEE



Current Status HTR

- Pre-prototype HTR board
  - 9U board, being worked on “as we speak”
  - Will have only 1 FPGA with full complement of associated parts
    - Xilinx XCV1000E
      - 400kbits BLOCK RAM
      - 900 pins, 660 user
      - 1.8Volts
    - Stratos dual LC receivers
      - Rated to 1.6Gbaud
      - 850 or 1300 nm
      - 3.3Volts
    - Deserializers
      - TI TLK2501 *TRANSCEIVER*
      - 8B/10B decoding
      - 2.5Volts
  - Internal use only



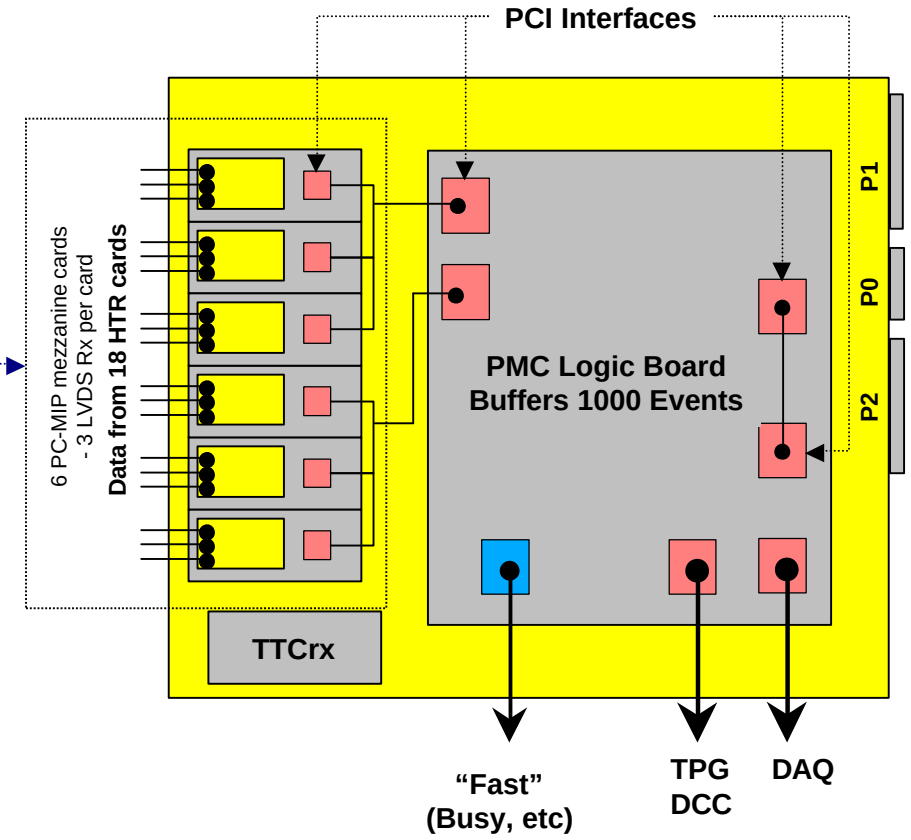
HTR Issues

- Opitcal link
  - Happy with the dual LC's – work well, available. No longer an issue
  - Front-END clock issues will be important for us.
  - O-to-E to deserializer work continuing
    - Need to have it understood soon…looks pretty good but not yet complete
  - Tracker Link? We will continue R&D until a decision…but we do not have much time left.
- Xilinx Vertex-II PRO
  - Internal deserializer. Very attractive advantages, integration and cost issues
  - Current schedule: Chips availble Q1 2002….we shall see
  - Current plan: we will stick with discrete components but will keep an eye on Xilinx PROs
- Testbeam 2002
  - Current prototype will need another iteration.
  - Next version will be used in Testbeam 2002.
  - Schedule calls for next iteration in Feb.
    - Tight schedule, but we think it'll work out ok.
- Energy filters still undefined
  - No impact on the schedule – we are waiting….

DATA CONCENTRATOR CARD

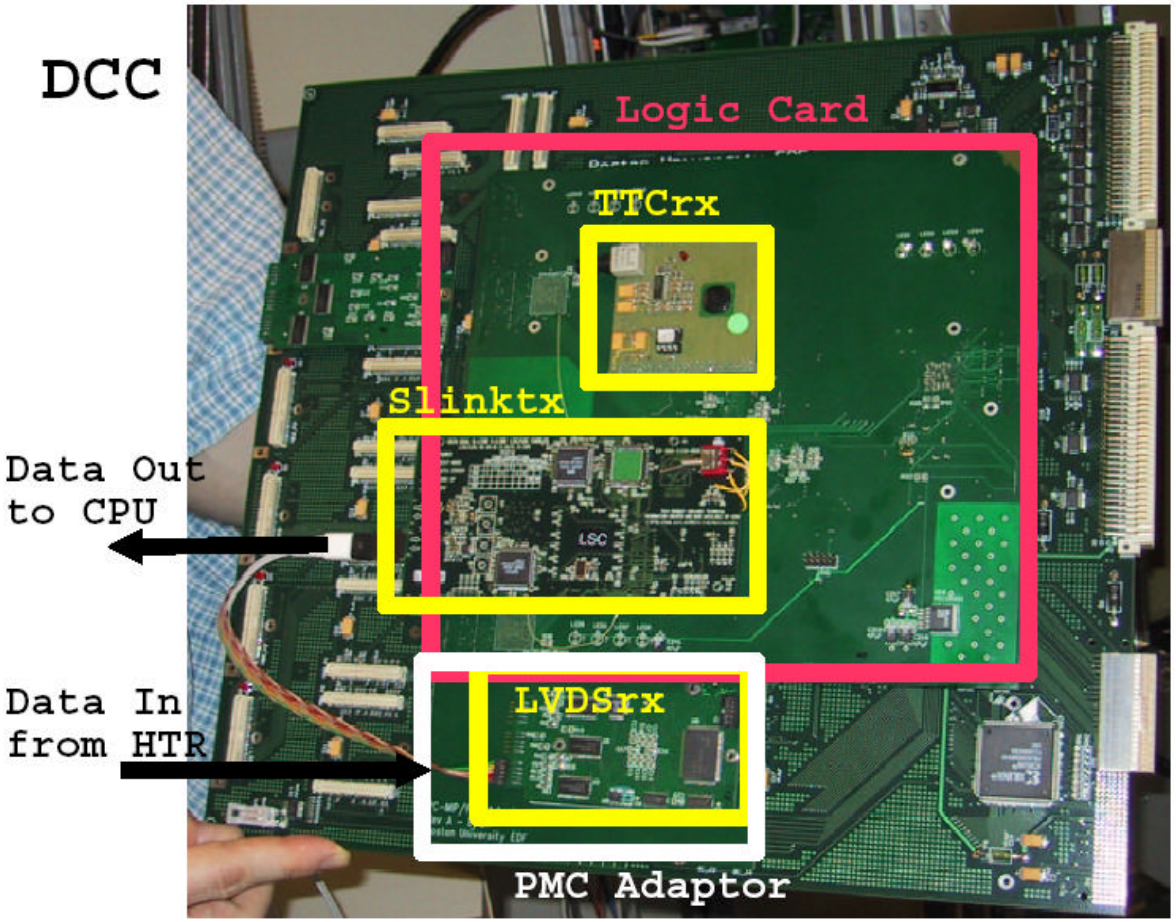
Motherboard/daughterboard design:

- Build motherboard to accommodate
  - PCI interfaces (to PMC and PC-MIP)
  - VME interface
- PC-MIP cards for data input
  - 3 LVDS inputs per card
  - 6 cards per DCC (= 18 inputs)
  - Engineering R&D courtesy of DÆ
- 1 PMC card for
  - Buffering
  - Output to TPG/DCC and DAQ
  - Fast busy, overflow, etc.
  - Giant Xilinx Vertex-2 1000 (XC2V1000)
- Transmission to L2/DAQ via S-Link



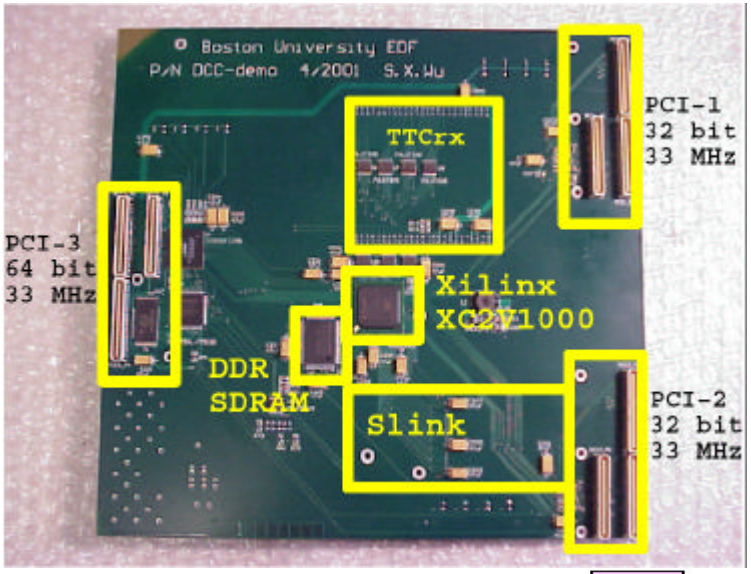
Current Status DCC Motherboard

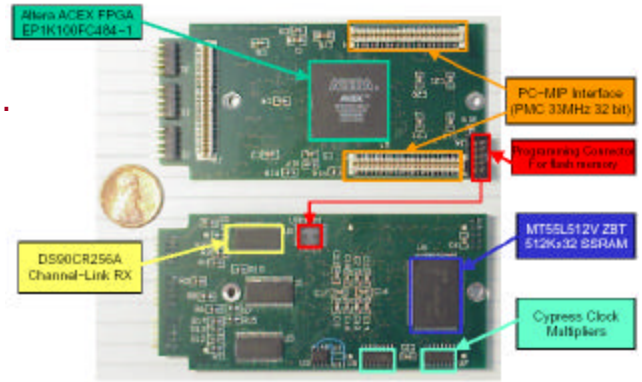
- Motherboard finished
  - 5 in hand for CMS.
- Production to start Q1 ’02
  - Piggyback on DZero order
- No real issues left

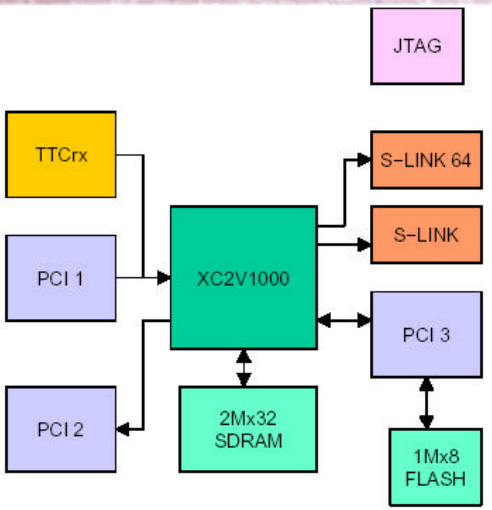


Current Status DCC Logic Board and LRBs

- Logic board
  - New version arrived, being assembled.
    - Parts for 3 available
  - Testing to start next week.
    - Working on event builder to send stuff to DAQ
  - Will have 2 S-Link connectors.
    - Raw data and TPG outputs
    - This prototype has only 1 now
  - Estimate for production: ~Fall 02
  - Issues:
    - DCC LB is daughterboard, has 2 granddaughter boards
      - Next will not have granddaughter boards, will be integrated
    - Input bandwidth measurements
- LRBs finished
  - Some software issues…



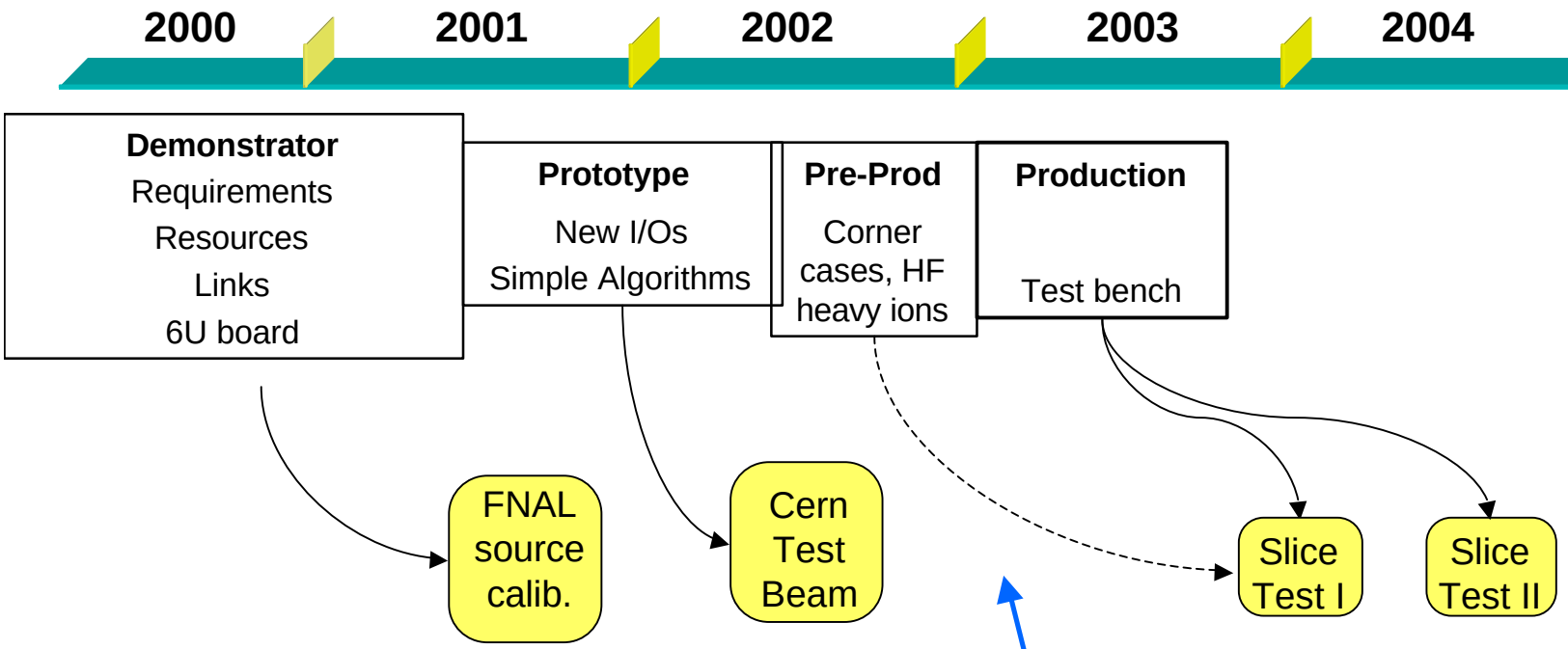




HCAL TIMING FANOUT Module

- Fanout of TTC info:
  - Both TTC channels fanout to each HTR and DCC
  - Separate fanout of clock/BC0 for TPG synchronization
    - “daSilva” scheme
- Single width VME module

Current Project Timeline



Pre-prod too short: not useful

Test bench before production ?

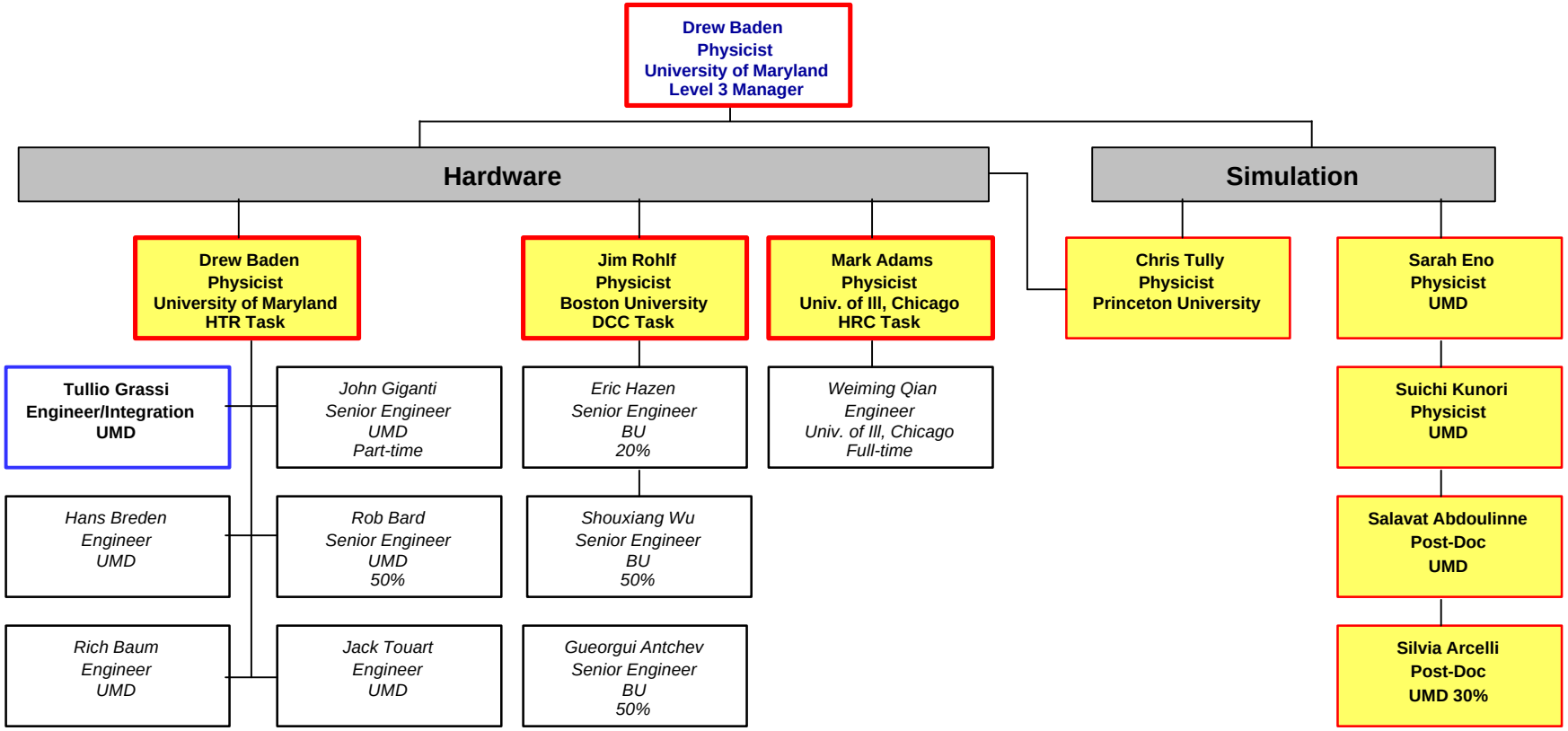
Slice Test I with pre-production ?

Vertex-2 PRO?

STILL SOME UNCERTAINTIES…

Manpower

- All Engineering/technical identified and on board.



Project Status Summary

- HTR (Maryland):
  - 6U Demonstrator built
    - 800 Mbps G-Links works fine
    - Integration with FEE and DCC complete
  - Tower mapping well in hand
    - Rohlf and Tully
  - 9U pre-Prototype underway
  - 9U Prototype layout underway
    - Plan to have this board on the test bench by Jan ’02
- “HRC”
  - Now the TTC fanout
  - First board being assembled
- DCC (BU)
  - DCC 9U motherboard built and tested ≡ finished
    - PCI meets 33MHz spec
    - Card is done!
  - Link Receiver Cards built and tested
    - Done
  - PMC logic board
    - First version complete
    - FPGA and etc. underway
- Crate CPU issues
  - Rohlf to lead
  - Tully is playing with BIT3 and DELL 3U rack mounted dual CPU