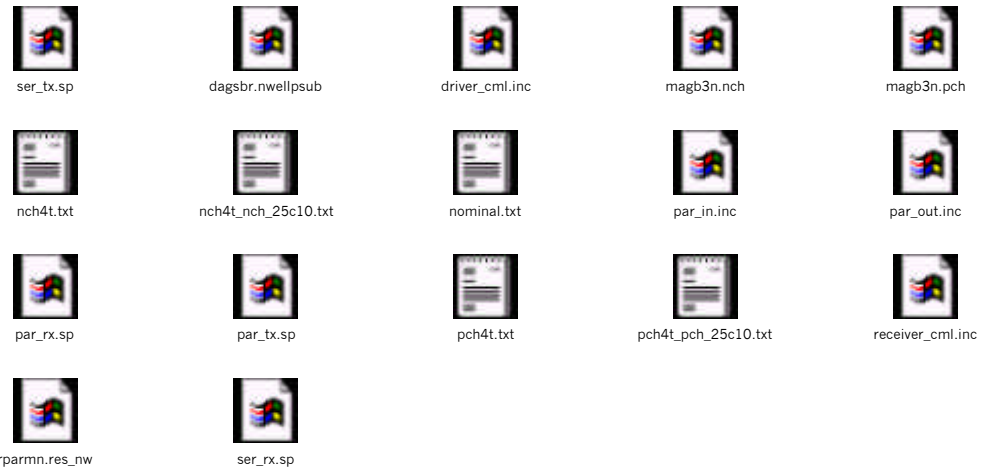
TLK2501 SPICE Models

Included are separate HSPICE models for the high speed TX, RX, and the low speed TX, RX parallel data buses. Documentation is included within the Spice netlist as far as connectivity. Files are as follows:



File:	Description
ser_tx.sp	Testbench for the CML outputs
driver_cml.inc	Subckt for CML outputs
ser_rx.sp	Testbench for the serial inputs
receiver_cml.inc	Subckt for serial inputs
par_tx.sp	Testbench for parallel inputs (TXD0:15)
par_in.inc	Subckt for parallel inputs
par_rx.sp	Testbench for parallel outputs (RXD0:15)
par_out.inc	Subckt for parallel outputs

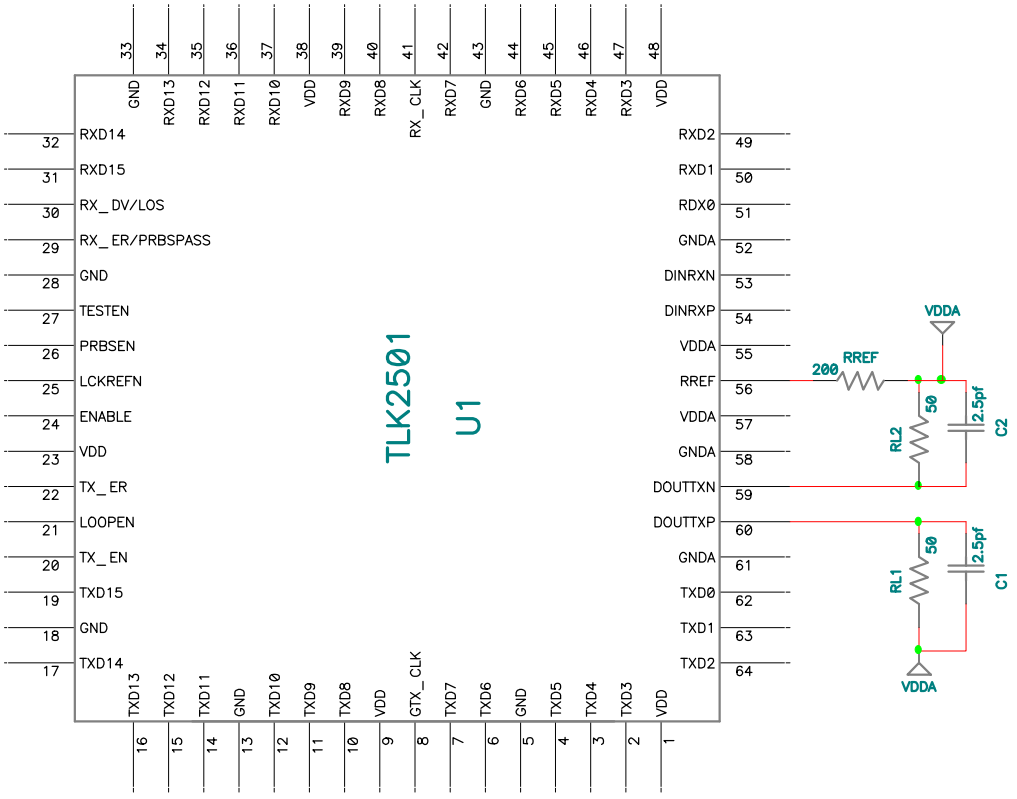
The other files are necessaries include files for the component model files.

Please note that these files are used for signal integrity analysis only and cannot be utilized to evaluate jitter.

High Speed Serial Test Bench

Transmitter:

TLK2501 High-speed serial driver CML driver test bench is the file listed as: **ser_tx.sp**
The signals DOUTTXN and DOUTTXP are the high-speed serial outputs represented as pins 59 and 60 in the data sheet. These signals are attached as two 50-ohm pull-up resistors and two 2.5pf test loads. The test load should be replaced with the customer's circuit to accurately simulate the system. The reference resistor is necessary to control the pre-emphsis and de-emphsis of the output signals(see the TLK2501data sheet for more detail. A circuit representing a portion of the Spice model is shown as below:



INPUT DATA

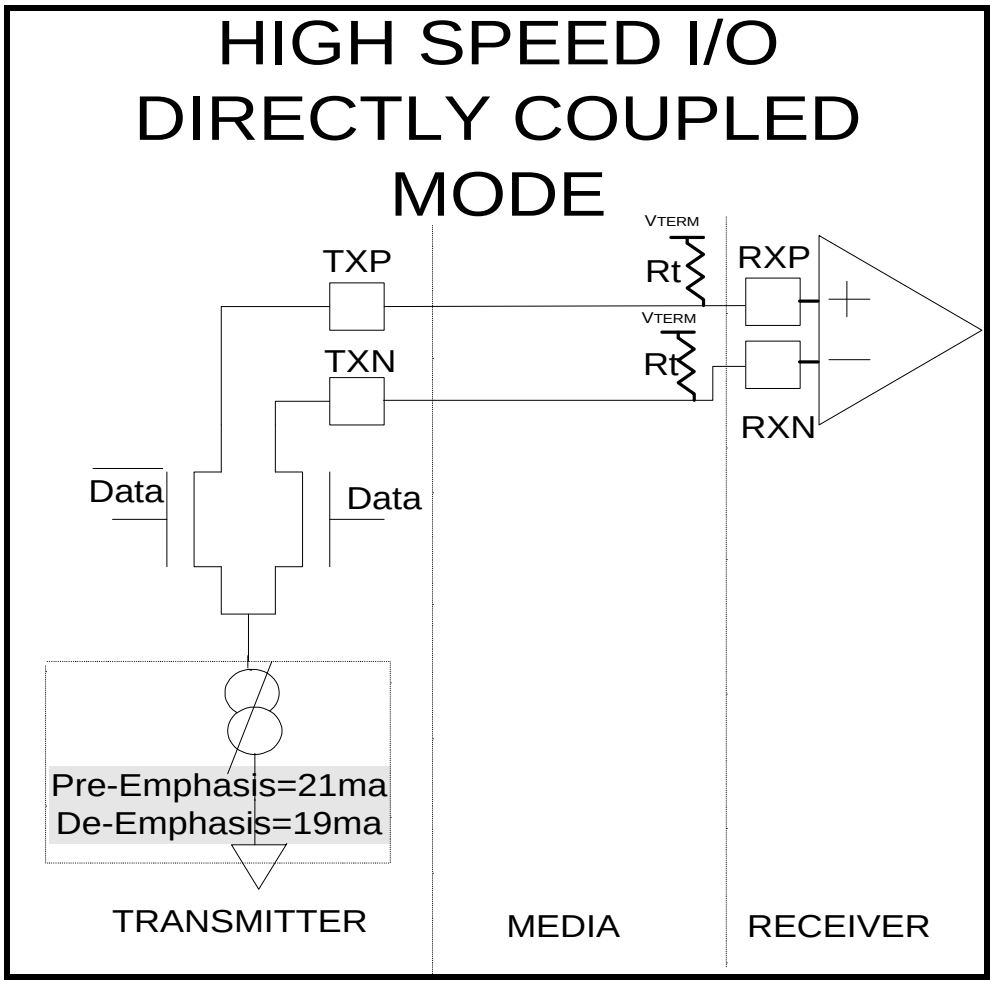
The **TXIN** and **TXINB** are the true and complement versions of the input signal. The example below is 0101 clock like pattern. However to check the pre-emphasis function, random data is preferred **TXINQ** and **TXINQB** should be the same data pattern as **TXIN** and **TXINB**, but delayed by a single clock cycle (1UI). This is required for the pre-emphasis function. Below is the sample-input statement:

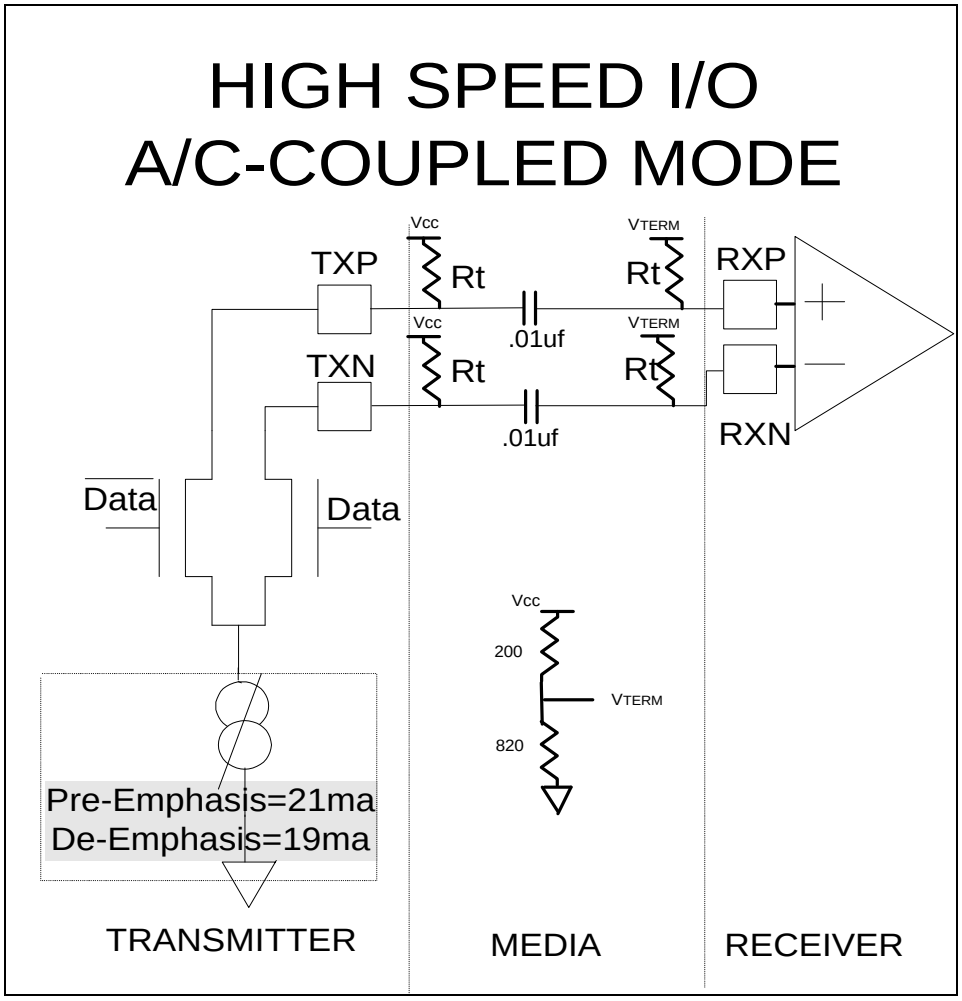
VTXP TXIN 0 PULSE 0 VDD (0n 0.1n 0.1n .27n .74n)
VTXM TXINB 0 PULSE VDD 0 (0n 0.1n 0.1n .27n .74n)
VTXPQ TXINQ 0 PULSE 0 VDD (.37n 0.1n 0.1n .27n .74n)
VTXMQ TXINQB 0 PULSE VDD 0 (.37n 0.1n 0.1n .27n .74n)

Receiver:

The high-speed serial stream is simulated in the **ser_tx.sp** test bench. The test bench termination resistors are configured in a way to achieve a proper swing and the customer may not choose to use this configuration if AC coupling the signal.

Possible Configurations




HIGH SPEED I/O
A/C-COUPLED MODE
Vcc
VTERM
TXP
Rt
Rt
RXP
Vcc
VTERM
.01uf
TXN
Rt
Rt
.01uf
RXN
Data
Data
Vcc
200
VTERM
820
Pre-Emphasis=21ma
De-Emphasis=19ma
TRANSMITTER
MEDIA
RECEIVER

Parallel Transmitter

In the spice model **par_tx.sp** the *GTX_CLK* parameter is the input clock signal. This signal has the same structure as the parallel TXD data inputs. Therefore, the customer can use the GTX parameter as a substitute for the TXD parameter. This is specified in the model structure:

```
** Parallel Input Source (Same structure applies for
** GTX_CLK/TXD inputs)
VCLK GTX_CLK 0 PULSE 0 VDD (0n 1n 1n 2.7n 7.4n)
```

Parallel Receiver

In the spice model **par_rx.sp** the parameter *RCLK* is the output recovered clock signal. This signal has the same structure as the parallel RX data outputs. Therefore, the customer can use the *RCLK* parameter as a substitute TXD parameter. This is specified in the model structure:

```
** Parallel Output Source (Same structure applies for
** RX_CLK/RXD outputs)
VCLK RCLK 0 PULSE 0 VDD (0n 1n 1n 2.7n 7.4n)
```