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For the HCAL Group:

• Boston University
• Fermilab
• Princeton University
• University Maryland
Overview

S-Link: 64 bits @ 25 MHz

READ-OUT Crate
- 1 PC Interface
- 12 HTRs
- 1 Clk board
- 2 DCC

20 bits @ 80 MHz = 1.6 Gbps FIBERS

FRONT-END Readout Box (RBX) On detector

Fibers

21-Jun-2005

HCAL TriDAS
HCAL VME Crate

- **VME Bridge module (CAEN)**
  - Configuration and monitoring over VME
- **Fanout module**
  - Receives TTC stream
  - Clones and fans out timing signals
  - Global HCAL synchronization w/RCT
- **HCAL Receiver & Trigger (HTR) module**
  - FE-fiber input, linearizers, filters...
  - Maintains pipeline
  - TP output via SLBs to RCT
  - DAQ output of raw/TP data to DCC
  - Spy over VME for monitoring
- **Data Concentrator Card (DCC)**
  - Inputs from HTRs
  - Output to DAQ
  - Generates busy if needed
  - Spy output via VME
HCAL Receiver & Trigger (HTR) (University of Maryland)
1. Receive HCAL data from front-ends
   • Synchronize optical links
   • Data validation and linearization
   • Form “trigger primitives” and transmit to Level 1 at 40 MHz
   • Pipeline data, wait for Level 1 accept
     – Upon receiving L1A:
       » Zero suppress, format, & transmit raw data to the concentrator (no filtering)
       » Transmit all trigger primitives along with raw data
       » Handle DAQ synchronization issues (if any)

2. Calibration processing and buffering of:
   • Radioactive source calibration data
   • Laser/LED calibration data

3. Support a VME data spy monitoring
HTR Schematic

- All I/O on front panel
  - Fiber digital data
  - Copper output to L1 and DCC
- FPGA logic
  - Fully programmable
HTR Rev 4

- Dual-LC O-to-E
- VME
- Deserializers
- Xilinx XC2V3000-4
- Stiffeners
- TTC mezzanine
- 6 SLBs
- 21-Jun-2005 HCAL TriDAS 7
HTR Status

• Goal: produce 270 Rev 4 HTRs by end of Summer 05

• Current status:
  – PCB manufacture complete
  – Boards are now being assembled, about 20/week
  – Checkout at Maryland, shipping to CERN
    • Currently about 70 boards at CERN
  – Will have plenty of HTRs to meet near term work needs
  – Will be ready for “Ready for Crates” this fall/winter
HTR Production

- Complete set of tests developed and being used at Maryland
- HTRs will be labeled, tested, cataloged, sent to CERN
- Will test at Maryland:
  - Basic operation (FPGA, Localbus, VME)
  - SLB connectivity
    - Will not test quality of clocking…
  - $10^{-12}$ BER optical test on all channels
    - Will use RBX if it arrives…otherwise will use emulator
Trigger Primitive Generation

- TPG firmware has been well simulated for ~2 years

150 GeV pion beam in HE

- TPG test performed during synchronous running in Sept 2004
  - Trivial identity LUTs for linearization
  - Form TPGs using simple peak algorithm
  - Readout raw data with corresponding TPG
  - Compare in time
HTR Firmware

- Firmware additions for latency issues
  - Asynchronous fifo changes from incoming clock phase to common
  - Will monitor fifo latency and report over VME and to DCC
  - Reset of fifo over VME
  - Will also reset fifo after loss-of-link recover (via FSM)
- Implemented data injection via VME into RAM
  - Will be useful for Level 1/HTR integration tests
- Work on zero suppression in progress
- Not yet working on the variety of summing for TPGs
  - HB vs HB/HE overlap vs HF
- Histogram firmware for HCAL sourcing done
- Battle tests – will be among many things tested in “slice” 06
Sources of variable latency:

- Each TTCrx has variable latency ~20ns
  - Varies chip-to-chip, voltage and temp dependent
- TLK2501 has variable latency
  - $76 < \Delta T < 107$ bit times, $3 < \Delta T < 6$ frames (20bit frames @ 80MHz)

Plan to track this:

- HCAL Front-end tools
  - Fast laser calibration pulses
  - TTC BC0 sent to FE, encoded into data stream
- HTR tools
  - SLB histograms

Beam in only 1 bucket at some time would be good

- Verification…
Activities in 904

- Test each HTR
  - Populate each card with 6 SLBs
  - Test with RCT receiver board
  - Validate clock, synchronization, quality…

- Populate VME crates with HTRs and store until November
  - Will have to wait for the SLBs
  - Current status has SLBs arriving en masse ~May?

- System testing, integration, commissioning…
  - We should push hard on SLB/RCT testing so that SLB firmware settles
HTR SLB Testing

- Maryland “sandwich” board
  - HTR and RCT Receiver are the “bread”
- Used to host RCT receiver to be able to test each link
- Status:
  - Prototype validated with RCT Receivers, no problems seen
  - Ready to use in bat 904
Fanout Card
(Princeton University)
Fanout Card

• All TPs from ECAL and HCAL associated with each LHC BX have to arrive at the RCT simultaneously
  – SLB mezzanine cards used by both ECAL and HCAL do this
  – But…SLB needs a global synchronous signal
  – Thus the need for a synchronous fanout module

• Built by Jeremy Mans and Chris Tully @ Princeton

• To be used for both ECAL and HCAL to implement synchronization
  – RX_CLK and RX_BC0 for SLBs
  – Also TTC stream and QPLL cleaned 80MHz clock for deserializer reference
Timing signals - Overview

Low-skew distribution tree for global BC0 and CLK (RX_BC0/RX_CLK)

Rack-to-Rack CAT 7

One fanout board per crate

HCAL VME Crates

TTC Minicrate

ECAL
RX_CLK and RX_BC0 Path

- Path is 3.3V differential PECL on Cat6 quad twisted pair
- RX_BC0 is generated from the FPGA decode of TTC broadcast on the global card

**Diagram:**
- TTC fiber
- RX_CLK, RX_BC0
- Cat6
- Fanout board in Global-mode
- Fanout board in Crate-mode
- TTCrx
- CLK40_Des1
- 3.3V CMOS
- QPLL
- FPGA
- RX_CLK
- RX_BC0
- TTCrx
- QPLL
- FPGA
- Max skew on HTR traces is 0.7 ns.

Spec is:
Skew < ±6 ns across HCAL and ECAL
Princeton Fanout Module
Fanout Status

- All PCBs remade with QPLL power fix
- Boards were assembled and are all being tested now
  - Initial tests were great – QPLL locked right away, stable…
- Should be able to ship full contingent to CERN in July
- Reminder: This will be used for both ECAL and HCAL
Data Concentrator Card (DCC) (Boston University)
DCC Status

- This card has been stable for several years
  - Tested under battle (see next slide)
  - Total number needed:
    - 32 for VME crates (2 per crate)
    - 6 spares
    - 12 for test stands

- Production status
  - 20 boards produced and ready for use
    - 4 already in the field and used extensively
  - Remaining 30 boards to be finished by the end of Sept 05
    - Waiting on parts…
HTR-DCC Testing

- **High rate tests completed in January 2005**
  - Ran at L1 trigger rules spacing (1 in 3, 22 in 2 orbits, etc…)
    - Equivalent to 30% occupancy, 7 samples per channel
  - Also ran at 200kHz with estimated 2xzero suppress size
    - Same event size – 4k fragments
    - Note: 20 time samples at full occupancy we saw the link backup as expected
      - Empty events seen, and after buffers flushed saw full events again
      - HTR/DCC link properly recovered!
  - Readout test with 128 consecutive events worked well
  - Bottom line
    - No problems with DCC as is, looks good to meet 100kHz 15% occupancy 7 time samples per channel

- **Ongoing firmware development**
  - DCC:
    - Improve error handling – nothing done there recently
    - New DCC libraries using HAL working fine thanks to Fernando
HCAL in general
HF Luminosity

• **Who:**
  – Maryland (Baden+Grassi)
  – Princeton (Marlow+Tully+asst prof)
  – Minnesota (Mans)
  – Virginia (Hirosky)

• **What:**
  – Produce instantaneous luminosity outside of DAQ path
    • No requirement on triggers, partitions, etc
  – Targets:
    • LHC machine
    • CMS “Luminosity database”
    • Control room monitoring
Luminosity Requirements

- 3654 bunches per orbit, 80% with beam

- Baseline proposal:
  - For each bucket calculate…
    - Sum $E_T$ over the 48 channels per HTR
    - Number of towers above $E_T$ thresholds (2 thresholds, 3 levels + active)
      - Energy in HF contained in 1 bucket….so TPG-like integration over buckets not needed
  - Send this info to daughter card on HTR every bucket
    - Daughterboard will keep histogram
  - R&D needed:
    - Requirements defined
    - Monte Carlo implementation
    - Live time considerations (hardware, software…)
    - Other
Hardware Implementation

• Prototype general purpose SLB replacement board built
  – Uses a single SLB-site
  – Embedded processor can store histogram over “n” orbits
  – Periodically send data to some computer using 100BaseT ethernet

• Will also be used for
  – Standalone triggering with Jeremy’s trigger board for SLICE
  – Testing SLB → Wisconsin Vitesse receiver link for production and installation
  – Can also be used for HO trigger with modest changes to above

• Status
  – Prototype produced, ethernet works, all ok
  – Lots of firmware development underway
  – Would like to try a significant test by end of 2005
Commissioning Tests

- Can we self trigger at P5 possibly this summer?
  - Yes using previously described mezzanine
    - Has RJ45 output specifically for H2 trigger board
    - Can cascade into simple 6U majority logic board Jeremy Mans built
  - New firmware for both HTR and mezzanine card tested
    - Scheme:
      - Use TPG path firmware, load LUTs correctly
      - Send 1 “muon” bit per TPG to sandwich board
      - Majority logic, send 1 bit to trigger board
      - Trigger board forms majority logic for trigger
Latency

- Definition: from BX to input to RCT
- Budget: 46 clock ticks
- Current best guess:
  - We are on the edge with almost no contingency
  - NOTE: HTR firmware not yet scrubbed…

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CCA can absorb some of the extra phase

46 clocks = 1,147.7 ns
Support Slides
Optical Attenuation and BER

“Typical setup”
- VECSEL transmitter, coupled to fiber via LC connector
  - Not locked, but fixed in place
- Fiber to LC to 8-way MTP male on HTR front panel
- Single fiber to LC connector for connection to STRATOS receiver

Output power:
- VECSEL advertised to put out 500µW (-3dBm)
  - Terry Shaw measured 570µW for a particular VECSEL
- UMD uses STRATOS LC transmitter
  - Advertised output 100-400µW (-4 to -10dBM)
  - Measured to be 90µW for a particular STRATOS
  - About 6dB below what we will use in CMS
  - Working on FE emulator now using GOL+VECSEL...

Attenuations measured:
- At each LC connector, 10 – 50% (0.5 to 1.5 dB)
- At MTP connector, same thing (.75dB advertised)
- Fibers are about ¼ dB per 100m
What do we need at the receiver to maintain link?
- Did a series of measurements with known attenuator
- Varied attenuation, looked at:
  - BER
  - TTL “signal detect” (SD) signal provided by Stratos part
- Found:
  - SD signal goes away when power is below about 2\(\mu\)W
    - Measured 1.5\(\mu\)W but accuracy of meter is probably \(\pm 0.2\mu\)W
  - BER climbs very fast right at this shoulder
- NB: achieved BER\(<10^{-15}\) with multiple fibers in parallel with crystals
Optical Attenuation (cont)

- Input power required to maintain link:
  - Measured failure for power < ~2\(\mu\)W (-33dBm)

- Power output by VECSEL:
  - 500\(\mu\)W output
    - Divide by 2 for digital averaging
    - Gives 250\(\mu\)W (-6dBm) output at source

- Expected Attenuations
  - Maximum of 8 couplings until the signal gets to the Stratos receiver on the HTR
    - 8x(0.5 - 1.5)dB = (4 – 12)dB
  - Add another ~1dB due to fibers

- Total power at inputs to HTRs:
  - -6dBm – (4-13)dB = -10 to -19 dBm
  - FNAL measured/calculated 7.3dB
    - Operating would be -13dBm

- We should have about 10dB margin
  - Probably more like 15dB
Longitudinal Separation Attenuation

- MTP connector ends are spring loaded into adapter
- Measured attenuation as a function of the separation
  - Separation should be ~0 if keys and adapters are working well
  - This should not be an issue for us (famous last words....)