GOL Startup Problem

Some users have reported a GOL startup problem that was confirmed by lab tests:
The GOL does not start properly if the clock signal is present before power on. What is critical about this condition is that a reset pulse is not able to restore normal operation.
For the chip to start correctly the clock signal must not be present at power up.

Possible solutions:

## First: (partial solution only)

The GOL contains two clock inputs: a differential input (LVDS) and single ended input (CMOS). In a system only one of these is used at a time. It is possible to use these inputs together with the clock selection signal to avoid the startup problem. The procedure is as follows.
1. At power off the inactive clock input is selected using the "selectDiff" signal;
2. Power is applied to the ASIC;
3. Select the active clock input using the "selectDiff" signal. At this point the GOL should work normally.

This is only a partial solution since this procedure will not be able to restore normal operation if the chip is already in a faulty condition.

Second: (system solution)

In a system to cycle the GOL power while maintaining the clock disabled might require to cycle also the power of several other components and/or systems thus imposing to the experiments a penalty that might not be acceptable. A second possibility is thus to add a power switch to control the GOL supply so that the GOL power can be cycled without interfering with other components in the system.
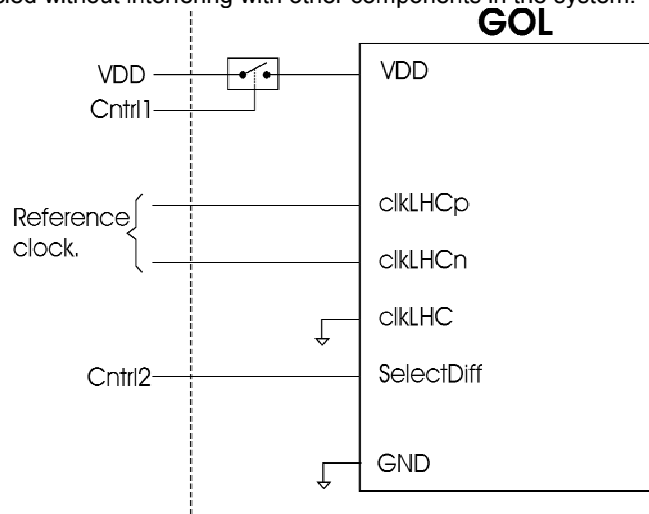
(Only relevant signals shown)

For example the figure above shows conceptually how this can be achieved. In that figure the LVDS clock inputs are used as the active clock input. A switch is used to control the GOL power. Two control signals are necessary: one to control the power switch and the other to select the clock source (depending on the implementation it might be possible to merge these two signals together). In the case shown in the figure, the operation is as follows:
   I. The single ended clock input is selected (that is, the non-active clock input is selected);
  II. The switch is turned off;
 III. The switch is turned on;
  IV. The differential clock input is selected (that is, the active clock input is selected).

This solution necessitates however the development of a radiation tolerant switch. However, this will not prevent the early development of boards using this configuration since the device pinout can be fixed. The boards can be tested even in the absence of the switch by a simple connection between the soldering input and output pads of the switch.

Third: (design revision)

It is possible to produce a reviewed version of the GOL were only the metal and via mask layers are changed to introduce the reset function on the PLL. This is of course the most costly solution but it is also the one that imposes no changes to the already designed systems that use the GOL ASIC.