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Extraordinary Mobility in Semiconducting Carbon Nanotubes

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ABSTRACT

Semiconducting carbon nanotube transistors with channel lengths exceeding 300 microns have been fabricated. In these long transistors, carrier transport is diffusive and the channel resistance dominates the transport. Transport characteristics are used to extract the field-effect mobility (79 000 cm^2/Vs) and estimate the intrinsic mobility (>100 000 cm^2/Vs) at room temperature. These values exceed those for all known semiconductors, which bodes well for application of nanotubes in high-speed transistors, single- and few-electron memories, and chemical/biochemical sensors.

Semiconducting carbon nanotubes have been proposed for such nanoelectronics applications as high-speed field-effect transistors (FETs),[1] few- or single-electron memories,[2] and chemical/biochemical sensors.[3,4] The charge-carrier mobility (i.e., conductivity normalized by the density of charge carriers) is crucial to each of these applications. Mobility determines the carrier velocity, and hence switching speed, in FETs. In floating gate memories and chemical/biochemical sensors, nanotube FETs (NT-FETs) will be used to detect charge, or a chemical signal converted to charge. Mobility determines the change in conductivity per charge, and hence the sensitivity of such devices. However, to date the mobility in semiconducting carbon nanotubes remains poorly understood. Estimates in the literature range from 20 cm^2/Vs (ref 5) to infinite, or ballistic,[6] and interpretation of device data has been complicated by short devices with non-Ohmic contacts.[7] In this letter we present measurements on extremely long (>300 μm), Ohmically contacted nanotube devices, showing that the field-effect mobility in semiconducting carbon nanotube transistors may be as high as 79 000 cm^2/Vs at room temperature, and the intrinsic mobility in semiconducting carbon nanotubes is even higher. These values exceed those of any other semiconductor at room temperature.

For this study we fabricated devices on degenerately doped (conducting) Si capped by t_{ox} = 500 nm of SiO_2 using the following method. Iron nanoparticles were deposited by first dipping the substrate into a solution of 30 μg/mL $Fe(NO_3)_3$ in 2-propanol[8] and then into hexane. Nanotubes were then grown in a tube furnace at 900 °C for 10 min using a mixture of H_2, CH_4, and C_2H_4 using the flow rates and following the method described in ref 9. After fabricating alignment markers with standard electron-beam lithography techniques, field-emission scanning electron microscopy (FESEM) at an acceleration voltage of 1 kV was used to locate the nanotubes.[10] The low acceleration voltage allows imaging of short nanotubes on an insulating substrate due to voltage contrast, and also reduces the possibility of e-beam damage to the nanotubes. The nanotube density was found to be about 30 short (~5 μm) nanotubes per 100 μm × 100 μm area and about 5−10 long (>100 μm) nanotubes per mm^2. As observed by other researchers, the long nanotubes are remarkably straight over a length of several hundred micrometers and aligned with the gas flow during growth.[11] Selected long nanotubes were contacted with Cr/Au contacts formed by electron-beam lithography. The contacts were not annealed after deposition. The electrical measurements were carried out by applying drain and gate voltages relative to the source electrode; the drain current was measured with an Ithaco 1211 amplifier. The amplifier rise time was set to 300 ms; no additional filtering of the data was performed.

Figures 1A and 1B show FESEM images of two nanotube FETs, NT1 and NT2. The contrast mechanism for this method of imaging[10] is based on differences in charging between nanotubes and the substrate; only the nanotubes which are electrically connected to the contact pads have large enough capacitance to be visible at this low magnification. While several (~15) short nanotubes are seen crossing the nanotubes under study, they do not form an extended electrical network. This was also verified by AFM imaging of smaller portions of the device.

Figures 1C and 1D show the low-bias conductance G of NT1 and NT2 as a function of gate voltage V_g at various

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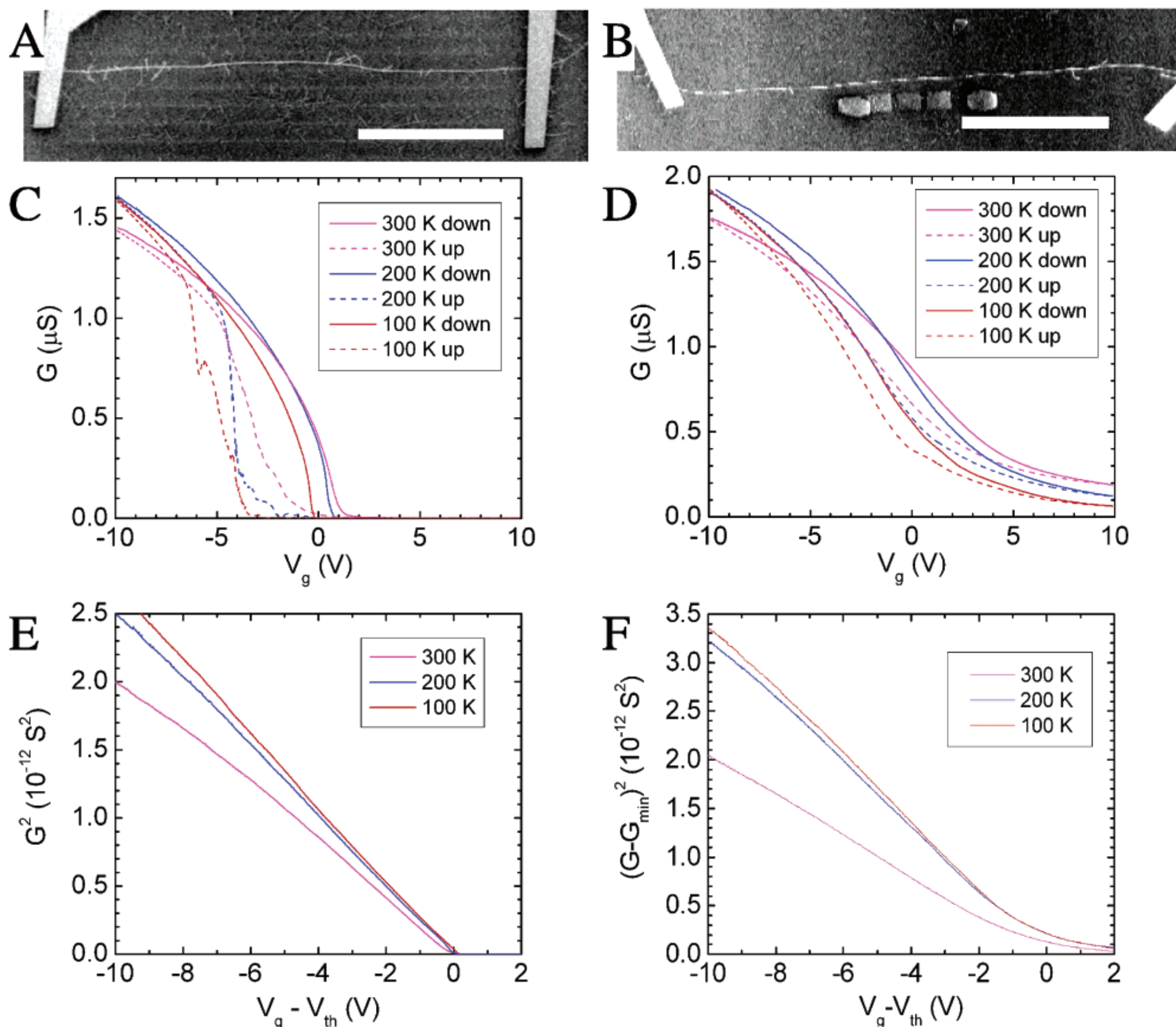

Figure 1. Ultralong semiconducting nanotube transistors. (A−B) Field-emission scanning electron micrographs of (A) NT1 (325 μm × 3.9 nm) and (B) NT2 (345 μm × 5.3 nm). Large white areas are Cr/Au source/drain contact pads; thin white lines are nanotubes. The scale bars are 100 μm long in (A) and (B). (C−D) Conductance of (C) NT1 and (D) NT2 as a function of gate voltage measured at a drain voltage $V_d = 50$ mV. Solid lines represent data taken on decreasing gate voltage, dashed lines taken on increasing gate voltage. (E−F) Conductance squared as a function of gate voltage minus threshold voltage for (E) NT1 and (F) NT2. A constant "metallic background" conductance $G(V_g = 10\text{ V})$ (see text) has been subtracted from the data for NT2 at each temperature. Fits to the relation $G^2 \propto (V_{th} - V_g)$ were used to determine the threshold voltage V_{th}.

temperatures measured in better than 10^{-5} Torr vacuum. Both devices show decreasing conductivity as the gate bias is made more positive, consistent with previous observations of p-type semiconducting behavior observed in similar, shorter devices.[1,5] Hysteresis is also evident in the $G(V_g)$, similar to that observed in shorter NT-FETs.[2] However, in these long NT-FETs, we observe that the downward sweep in gate voltage is typically smoother and more reproducible than the upward sweep. This hints that the trapped charges responsible for the hysteresis are positive (holes), with few trapped holes on the downsweep, and many trapped holes, in irreproducible configurations, on the upsweep. We therefore use the downsweep in V_g for our analysis in further sections.

Device NT1 turns off completely as the gate voltage becomes positive, while the conductance of NT2 tends to a low finite value, which decreases strongly with decreasing temperature. We hypothesize that NT1 is either a semiconducting SWNT or a multiwalled nanotube (MWNT) consisting of a few semiconducting shells, while NT2 is a MWNT with a semiconducting outer shell, and at least one metallic inner shell. Thus as the gate voltage becomes positive, most of the conductance of NT2 is suppressed as the outer shell is depleted of holes, but there is residual conductance through an inner metallic shell.[12] We can account for this extra "metallic background" conductance by subtracting the conductance measured at $V_g = 10$ V from the entire data set.

Figures 1E and 1F show the conductance squared as a function of gate voltage for NT1 and NT2 at various temperatures. The "metallic background" has been subtracted from the data for NT2. We observe that the data closely follow the relationship $G \propto (V_{th} - V_g)^{1/2}$. We assume that

V_{th}, the voltage where G tends to zero, is the threshold voltage for our NT-FETs. With variations in the threshold voltage and the presence of a parallel metallic channel in NT2 accounted for, the $G^2(V_g)$ data for NT1 and NT2 (Figures 1E and 1F) agree very well, indicating that the conductance mechanism is similar for both nanotubes. We also note that other similar length nanotube devices with smaller diameters have been studied; these devices showed conductance and transconductance values of magnitude comparable to the devices here (indicating comparable field-effect mobilities − see below). However, the hysteretic effects were larger and less repeatable. For the remainder of the letter we will analyze the data only for sample NT1. Similar conclusions can be drawn from device NT2 and other devices.

It is notable that the conductance of NT1 at $V_g = -10$ V exceeds 1.4 μS at room temperature. Assuming *zero* contact resistance, this conductance corresponds to a one-dimensional conductivity σ of 4.6×10^{-8} S·cm. If this nanotube is single-walled, or multiwalled with the current largely carried by the outer wall at low bias,[12] then the electronic mean-free-path l is given by $\sigma/2G_o = 2.9$ microns, where G_o is the conductance quantum, approximately 77.5 μS. Finite contact resistance would imply a larger σ and, thus, a larger l. The results imply that at large gate voltages, semiconducting nanotubes may achieve electronic mean-free-paths similar to those of metallic nanotubes.[13] Note that the cross-sectional area of the nanotube may be divided by the one-dimensional conductivity to obtain a three-dimensional resistivity: $\rho_{3D} = A/\sigma = 2.6\ \mu\Omega$-cm. The striking result is that the nanotube conductivity may be tuned from insulating to comparable to good metals. Similar conclusions would be reached for the semiconducting contribution to the conductance of NT2.

The above results argue strongly that the measured resistance in our devices is dominated by the channel resistance, not the contact resistance; the inverse would imply an unphysically high mean-free-path in the channel. However, it is not clear that the channel resistance dominates at all gate voltages; the turn-off of the device at threshold could be governed by a different mechanism, e.g., Schottky barriers at the contacts. It has been shown that some nanotube transistors are dominated by Schottky barrier contacts,[7] while Ohmic contacts may be achieved under other conditions.[6,14] To investigate the nature of the contacts, we examine the subthreshold behavior of the conductance of NT1.

Figure 2 shows the subthreshold behavior of NT1. The subthreshold swing S, equal to $(d(\ln G)/dV_g)^{-1}$, is small (~120 mV/decade at 100 K) and temperature-dependent, in fair agreement with the standard MOSFET model and the value reported in ref 6, but not with the Schottky barrier model which predicts a large (~1000 mV/decade), temperature-independent subthreshold swing.[7] We conclude that the contacts are Ohmic (or at least any Schottky barrier present has conductance much higher than the channel conductance); the resistance is dominated by the intrinsic resistance of the nanotube channel at all gate voltages.

We now discuss the mobility $\mu = \sigma/q$ of our nanotube devices. In one dimension $\sigma = GL$ is the conductivity, where G is the conductance and L the length of the device. The

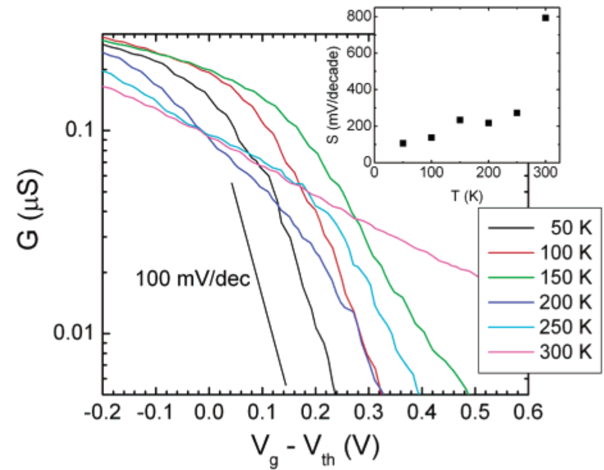

Figure 2. Conductance of NT1 as a function of gate voltage at various temperatures in the subthreshold region of the semiconducting nanotube transistor. The straight line indicates a subthreshold swing S of 100 mV/decade. The inset shows the subthreshold swing S as a function of temperature.

charge density per length q on the nanotube is given by $q = c_g(V_{th} - V_g)$ with c_g being the capacitance per length, V_{th} the threshold voltage at which the device turns on, and V_g the applied gate voltage. Note that in order to ensure that the charge density is uniform the device length must be significantly greater than the charge screening length, which in one dimension is roughly given by the dielectric thickness; this condition is easily satisfied for our devices with $L >$ 300 μm and $t_{ox} = 500$ nm. The mobility is then given by

$$\mu = \frac{L}{c_g} \frac{G}{(V_{th} - V_g)} \tag{1}$$

This definition is analogous to the "effective mobility" for conventional FETs.[15] Since it is hard to define V_{th} unambiguously, studies of conventional FETs often use the so-called "field-effect mobility" μ_{FE} to compare device properties. The field-effect mobility is device-specific, not material-specific, and includes effects such as contact resistances, surface effects, etc. Adapted for the dimensionality of a nanotube device it can be calculated by

$$\mu_{FE} = \frac{L}{c_g} \frac{\partial G}{\partial V_g} \tag{2}$$

This definition agrees with the initial one if the mobility does not depend explicitly on V_g, i.e., G is proportional to $V_g - V_{th}$. Typically (and in our case) G is sublinear in $V_g - V_{th}$, and μ_{FE} underestimates the mobility.

From a commercial computer simulation we obtain the electrostatic gate capacitance $c_{g,el} = 190$ fF/cm for NT1. (Note $c_{g,el}$ is significantly smaller than the 360 fF/cm obtained from the oft-used analytical formula for a cylinder over a plane in an infinite dielectric medium, due to the absence of dielectric above the nanotube.) The electrostatic gate capacitance is also significantly less than the quantum capacitance $c_q = e^2D > 4$ pF/cm where D is the density of states

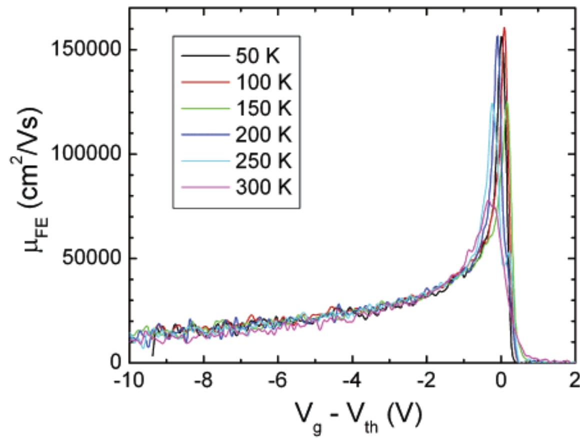

Figure 3. Field-effect mobility (defined in text) at various temperatures for NT1.

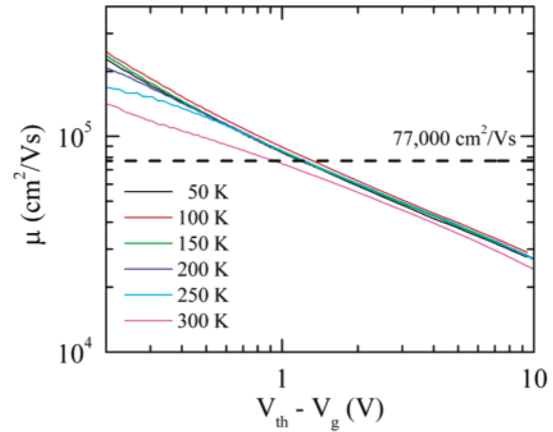

Figure 4. Intrinsic mobility of the semiconducting nanotube transistor as a function of gate voltage at temperatures 50 to 300 K. Note that for gate voltages below 1 V the mobility at 300 K exceeds the room-temperature Hall mobility of high-purity InSb[18] (77 000 cm^2/Vs).

per length. (Quantum capacitance relates the charge to the shift in the chemical potential of the nanotube). The capacitances add inversely; the total capacitance is given by $c_g = (1/c_{g,el} + 1/c_q)^{-1}$, so the much larger quantum capacitance may be ignored[16] and $c_g \approx c_{g,el} = 190$ fF/cm.

In analyzing our data, we will first calculate the field-effect mobility μ_{FE}, since it is unambiguous − independent of the choice of V_{th}. The field-effect mobility is technologically relevant; it gives a measure of the transconductance of the device and is important in determining the sensitivity of the device to changes in gate voltage and/or charge, which ultimately determines the sensitivity of chemical sensors or floating gate memories.

Figure 3 shows the field-effect mobility for device NT1 for different temperatures. The curves show a peak due to the sublinear dependence of $G(V_g)$. At 300 K the curve peaks at 79 000 ± 8000 cm^2/Vs, where the error represents the uncertainty in the gate capacitance. We are not aware of a higher field-effect mobility achieved at room temperature in any other type of semiconductor device. For comparison, field-effect mobilities achieved in silicon MOSFETs are less than 1000 cm^2/Vs (ref 17).

We next estimate the intrinsic mobility μ of the nanotube channel, given by eq 1, using the threshold voltage determined earlier from the fit to $G \propto (V_{th} - V_g)^{1/2}$. Figure 4B shows the mobility μ as a function of V_g. (Because of the uncertainty in the determination of the threshold voltage, we do not assign significance to the details of the curves for $V_{th} - V_g < 0.2$ V.) The mobility roughly follows a power-law dependence on V_g, with an exponent of −1/2, as expected since $G \propto (V_{th} - V_g)^{1/2}$. For $V_{th} - V_g < 1$ V, the mobility exceeds the previously reported highest mobility in a semiconductor at room temperature, 77 000 cm^2/Vs, the Hall-mobility of InSb.[18] Note that a similar calculation for NT2 would give similar results, except near the threshold where the effect of the extra metallic conductance cannot be properly evaluated.

We now turn to the high-electric-field behavior of the device. Figure 5A shows the drain current as a function of drain voltage $I_d(V_d)$ of NT1 at various gate voltages at 1.5 K. As for a conventional FET, saturation of the drain current is evident when $V_d \approx V_g - V_{th}$. We obtain the saturation current $I_{d,sat}$, from the intersection of linear fits to the low-bias (Ohmic) region and high-bias saturation region (see Figure 5A). The current saturation in MOSFETs at high bias voltages allows an independent estimate of the mobility. This

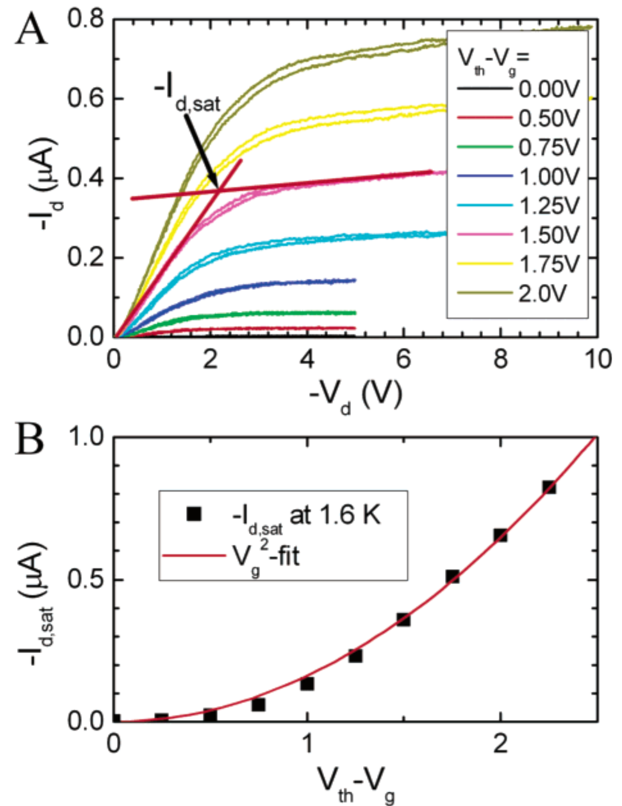

Figure 5. Determination of the saturation mobility. The saturation current $I_{d,sat}$ is determined from the drain current-drain voltage ($I_d - V_d$) curves using the intersection of linear fits to the low-bias region and the saturation region. Sweeps toward negative V_d and back to zero are shown, with negligible hysteresis (A). The dependence of $I_{d,sat}$ on V_g is roughly quadratic, as expected in the conventional MOSFET model (B).

so-called saturation mobility μ_{sat} (corrected for the dimensionality of a nanotube transistor) is given by the following relation:[15]

$$\mu_{sat} = \frac{2L}{Bc_g} \frac{|I_{d,sat}|}{(V_{th} - V_g)^2} \tag{3}$$

where $I_{d,sat}$ is the saturation current and B is the so-called body factor, which is not well understood even for a traditional MOSFET, but is typically of order unity. For this reason the saturation mobility can only be an order-of-magnitude estimate used to corroborate the general validity of the previous calculations. From Figure 5B, $|I_{d,sat}|/(V_{th} - V_g)^2 = 160$ nA/V^2. With $B = 1$ we obtain $\mu_{sat} = 55\,000$ cm^2/Vs, which is in good agreement with the calculations presented above. This agreement is further evidence that our long nanotube transistor may be described within the diffusive MOSFET model. We note that because of the length of our device, the electric fields studied here are an order of magnitude smaller than those predicted for velocity saturation in an NT-FET,[19] thus the saturation mobility obtained here still reflects the low-field mobility.

A microscopic theory to explain the behavior of the intrinsic mobility is lacking. However, the fact that it is largely temperature independent and has a simple power-law dependence on the gate voltage V_g (and hence the charge density q) is suggestive that scattering by charged impurities dominates the resistance for most temperatures and gate voltages (the dependence of effective mass, density of states, and Fermi energy on q are significantly more complicated, and hence the dependence of mobility on these quantities does not show any simple behavior). An estimate of the mobility of 120 000 cm^2/Vs at room temperature and zero doping has been obtained from calculation of the electron−phonon scattering for a 4.6 nm diameter zigzag-nanotube.[19] This result agrees quite well with our observed reduction in the mobility at 300 K; the temperature dependence is most pronounced when the mobility is near 100 000 cm^2/Vs, suggesting that at low $V_{th} - V_g$, phonon scattering is limiting the mobility. While the apparent temperature dependence at large negative gate voltages may be due to the larger hysteresis at room temperature, the dependence at small gate voltage cannot be explained by hysteresis, since the hysteresis is negligible near zero V_g, and the reduction in conductance would imply *less* hysteresis at higher temperatures. It is interesting to note that the mobility of holes in bulk graphite at room temperature is quite high, 15 000 cm^2/Vs (ref 20). However, graphite is semimetallic, not semiconducting, so bulk graphite field-effect transistors cannot be realized. The nanotube may then be viewed as a way to engineer a band gap in this high-mobility material.

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