Nanotubes are High Mobility Semiconductors

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Abstract. The electron transport properties of a very long (20 micron) CVD-grown nanotube are reported. In this device the transport is dominated by intrinsic scattering processes at room temperature. The room temperature hole mobility is 20,000 cm^2/Vs, exceeding that of technologically-relevant semiconductors. The mobility increases with decreasing temperature, and is estimated to be greater than 180,000 cm^2/Vs at 470 mK.

Single-walled carbon nanotubes (SWNTs) are currently being considered for revolutionary applications in nanolectronics. While metallic SWNTs have been shown to conduct electrons ballistically over micron lengths at room temperature, the picture of electron transport in semiconducting SWNTs is less clear. Transport in semiconducting SWNTs synthesized via laser ablation has been previously interpreted as diffusive, with a low mobility (~20 cm^2/V·s) [1]. However electrostatic force microscopy (EFM) [2] and low temperature transport [3] measurements on similar devices indicate that the conduction is limited by a series of large transport barriers. EFM measurements on semiconducting SWNTs grown by chemical vapor deposition instead show diffusive conduction with a long mean free path. Here we study electron transport in a very long (20 micron) CVD-grown semiconducting nanotube, in which we expect the resistance to be dominated by intrinsic scattering processes in the nanotube, and not the contacts. An extremely high mobility is observed, 20,000 cm^2/V·s at room temperature, greatly exceeding the hole mobilities of current semiconductor MOSFETs. The mobility increases with decreasing temperature, indicating that a temperature-dependent scattering process dominates at room temperature.

The nanotube studied here was synthesized by chemical vapor deposition (CVD) using a method adapted from Hafner et al. [4]: The starting substrate is degenerately-doped silicon with a 500 nm oxide layer. Catalyst is deposited by dipping the substrate into a $Fe(NO_3)_3$/isopropanol solution followed by dipping in hexane to form $Fe(NO_3)_3$-nanoparticles on the surface. The catalyst is first reduced in flowing H_2-gas at 900 ºC, followed by CVD of nanotubes using pure methane as the feedstock. A porous alumina substrate coated with an iron/molybdenum catalyst [5] placed upstream from the samples was found to promote nanotube growth.

After growth, Cr/Au alignment marks are patterned on the substrate using a standard electron-beam lithography process. Nanotubes are located relative to the alignment marks with an atomic force microscope (AFM). A second electron-beam lithography step establishes Cr/Au source and drain contacts to the nanotube for conductance measurements. The conducting silicon substrate acts as a third (gate)
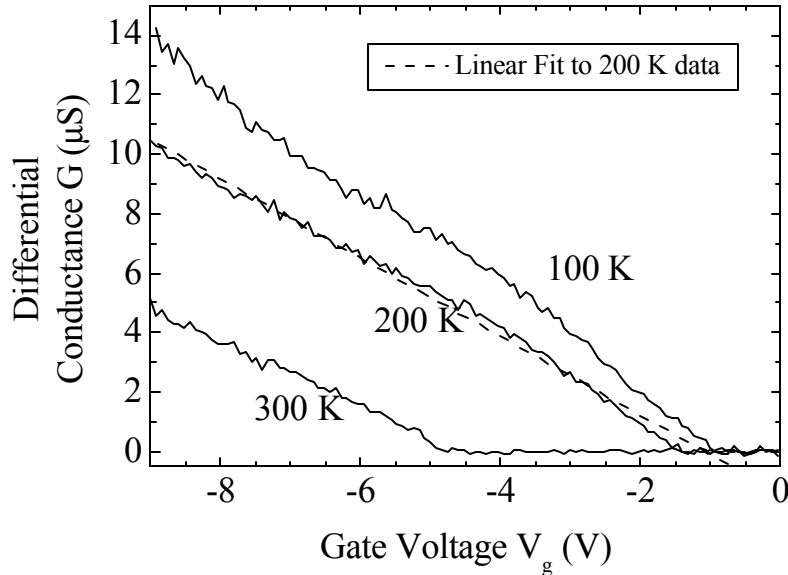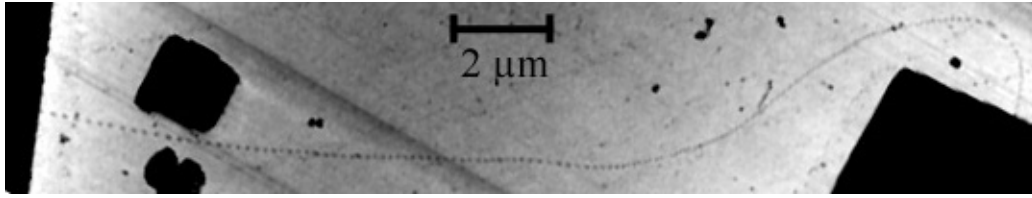
FIGURE 1. Atomic force micrograph (upper panel) of the device discussed in the text. The thin grey line is the nanotube, the large dark areas are Cr/Au pads. The nanotube has a length of ~20 microns between electrodes, and a diameter of 2.2 nm. The lower panel shows the differential conductance at zero DC-bias voltage as a function of the applied gate voltage measured at various temperatures.

electrode. Conductance measurements were made in the linear response regime using an AC technique.

Figure 1 (upper panel) shows an AFM topograph of the device. The thin curving nearly horizontal line is the nanotube, the large dark blocks are Cr/Au electrodes and alignment markers. The nanotube has a diameter of approximately 2.2 nm. The lower panel of Figure 1 shows the conductance of the device as a function of gate voltage. As previously observed before [1, 6] the semiconducting nanotube behaves similarly to a p-channel field effect transistor (FET).

The characteristics of an FET allow us to calculate the mobility of the majority carriers (holes in a p-channel FET) using the slope dG/dV_g of the linear part of the conductance vs. gate voltage curve as shown in Figure 1. For a nanotube FET this yields the following formula for the mobility μ:

$$m = \frac{L}{c_g} \frac{dG}{dV_g}.$$

Here L is the length of the nanotube and c_g is the capacitance per length between the nanotube and the gate. We determine this capacitance (approximately 69 e⁻/V·μm) from the Coulomb oscillations measured in metallic nanotubes on the same substrate.

For the 20 μm long nanotube shown in Figure 1 room-temperature mobility is 20000 cm^2/Vs. This exceeds the hole mobility for all typical semiconductors and is only comparable in magnitude to the in-plane hole mobility in high quality graphite crystals, 15000 cm^2/Vs [7].
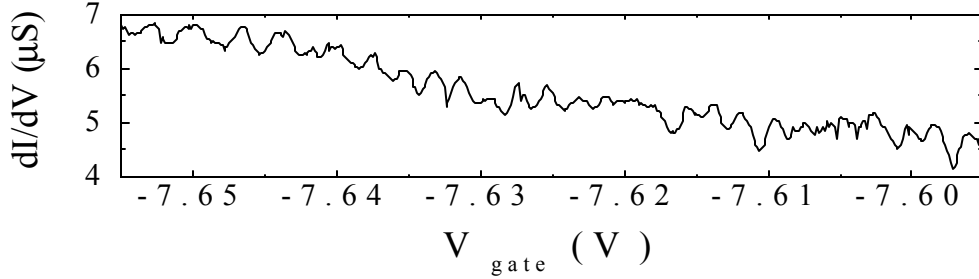
The differential conductance as a function of gate voltage was measured at various temperatures from 470 mK up to room temperature. As shown in Figure 1, the behavior remains roughly linear, allowing the temperature dependence of the mobility to be extracted down to a temperature of ~40 K. (At lower temperature the conductance fluctuates due to incipient Coulomb oscillations.) The results are shown in Figure 2. The mobility increases slowly as temperature decreases, and appears to saturate at ~30,000 cm^2/Vs at approximately 100 K. The increase in mobility indicates that we are probing an intrinsic process; we expect that a Schottky barrier or other tunnel barrier at the nanotube-electrode interface would have a decreasing or constant conductance as the temperature is lowered. However, the saturation of the mobility may indicate the point at which the contact resistance begins to dominate the measured resistance. The temperature dependence suggests the scattering arises from electron-electron or electron-phonon interaction, however the exact mechanism is not yet clear. Phenomenologically, the log-log plot in Figure 2 suggests a $T^{-0.4}$ power law behavior
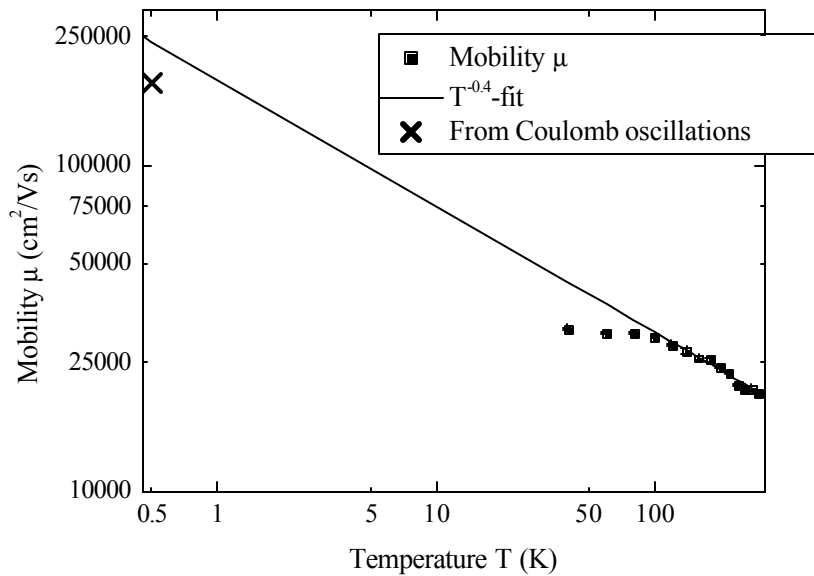
FIGURE 2. Temperature dependence of the hole mobility. The power law fit has been calculated from the data points between 120 K and 300 K. The low-temperature value at 470 mK has been determined using the periodicity of Coulomb oscillations, and should be treated as a lower bound.

for the mobility above 120 K.

The mobility may be estimated in a different way at low temperatures. At 470 mK, we observe regular oscillations in the conductance as a function of gate voltage (see Figure 3), which we interpret as Coulomb oscillations with a very small charging energy, comparable to the thermal energy. This behavior is in sharp contrast to that observed in laser-ablation grown nanotubes, which exhibit a gap in the conductance as a function of source-drain voltage, interpreted as due to a series of large tunnel barriers approximately 100 nm apart [3]. Using the capacitance per length mentioned earlier, we estimate that the oscillations are associated with a quantum dot of length at least 10

FIGURE 3. Coulomb oscillations in the differential conductance at zero DC-bias of the 20 μm long nanotube measured at 470 mK.

microns. Assuming that the mean free path L is at least half this length (5 microns) we determine the mobility as follows:

$$\boldsymbol{m} = \frac{eL}{m^* v_f} = \frac{eL}{\hbar k_f}, \text{ with } k_f = \frac{\boldsymbol{p}}{4} n = \frac{\boldsymbol{p}}{4} \frac{c_g (V_g - V_t)}{e},$$

where n denotes the linear carrier density, $\hbar$ Planck's constant, k_f the Fermi wavenumber, m^* the effective hole mass, V_g the gate voltage, and V_t the threshold voltage (or turn-on voltage) of the device. With V_g-V_t = 8 V, the mobility is 180,000 cm^2/Vs. We believe this is a lower bound for the low-temperature mobility of the device. Interestingly, this estimate is quite consistent with the power-law increase in mobility observed at high temperature (see Figure 2).

In conclusion, we have shown that CVD-grown single-walled carbon nanotubes have exceptionally high hole mobilities at room temperature, rivaling the best known semiconductors. This result is very promising for the use of semiconducting SWNTs in applications such as field-effect transistors or memories. Our results also provide the first glimpse into the intrinsic scattering mechanism in SWNTs.

ACKNOWLEDGEMENTS

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